Prime Computer Logic Diagrams

ASYNCHRONOUS MULTILINE CONTROLLER

A.M.L.C. E.V.

LOGIC DIAG. LDS1630

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DWG.NO.	DATE	REV.
LDS1630	6/24/77	B

MATERIAL FOR AMLC MANUAL

(Models 5002, 5004, 5052, 5054, 5075)

MATERIAL FOR AMLC MAINTENANCE MANUAL
(Covers Models 5002, 5004, 5052, 5054, 5075)

1. GENERAL

The AMLC will interface 8 or 16 full-Duplex Asynchronous communication lines to a PRIME CPU (100, 200 or 300). The following models are currently available:

5002 - 8 line with full data set control

5004 - 16 line with full data set control

5052 - 8 line with limited data set control for direct connect

5054 - 16 line with limited data set control for direct connect

5075 - 8 line 20 ma current loop and 8 line with limited data set control for direct connect

NOTE: Except for the 20 ma current loop interface, all interfaces conform to RS232C EIA spec.

Full data set control means four control signals and four status signals per line.

Limited data set control means one control signal and one status (or sense) signal per line.

The AMLC will have the following functional characteristics:

- Interfacing to the central processor will be via the programmed I/O, priority interrupt and direct memory transfer.

- Will control eight or sixteen full or half duplex asynchronous communications lines.

- Line speeds up to 19,200 baud.

- Eight different line speeds per controller. Of these eight, four are fixed at 110, 134.5, 300 and 1200 baud. A fifth clock can be specified by the user. This clock is generated by the overflow from a preset 12 bit counter. The preset is implemented by a software loaded register.

  The remaining three clocks can be jumper selected by the user from the following speeds: 75, 150, 600, 1800, 2400, 4800, 9600, and 19,200 baud. Default selection is 75, 150, and 1800.

- Each line will have the following software controllable line parameters:

  1 of 8 clock speed

  5, 6, 7 or 8 bit character length

  Even, Odd, or No Parity

  1 or 2 stop bits

  Loop line

- The following line control functions will be under software control on a per line basis:

  Enable/Disable Transmit
  Enable/Disable Receive
  Disable Receiver but report open line (break)
  Echo back Received Data Enable/Disable
  Interrupt every character time Enable/Disable

  } by I/O Instruction

  Transmit Line Break
  Transmit Line Mark

  } by means of control bits with Transmit Character

- Data Set Interface

  An EIA RS232-C/CCITT V24 compatible interface is provided on each line. The following signal lines are provided:

  a) Transmit Data

  b) Receive Data

  c) Signal Ground

  d) Data Set Control Bit. Useful for EIA interface peripherals, i.e., line printer, CRT, etc.).

  e) Data Set Sense Bit

2. PHYSICAL DESCRIPTION

The AMLC models 5052, 5054 and 5075 each consist of one 15" X 16" PRIME board. The AMLC can be inserted in any slot in the I/O bus.

The AMLC models 5002 and 5004 consist of one AMLC board and one DSC board.

3. OUTLINE DESCRIPTION

The AMLC is shown in Figure 1. The main component parts are:

a) RIORF

This is a 16 X 16 RAM used as registers for the:

1) Interrupt Vector Address

2) DMA/DMC Channel Address

3) DMT Address (Bits 13-16 come from line number).

b) AMLC Status Register

This is a combination of registers and individual flip flops which can be interrogated by an INA 0754 to ascertain AMLC status.

c) RAMC

This is an 8 X 16 RAM. One memory location is allocated per line for the following control bits:

1) Transmit Enable

2) Receive Enable

3) Receive Off Report Open Line

4) Echo Mode

5) Enable Character Time Interrupts

d) RD Register

This is a 16 bit register. It is used as temporary storage of 1) transmit character from CPU before they are transferred to the UART in the line logic, 2) line control bits to be written into RAMC and 3) line configuration bits to be transferred to the UART.

e) Clocks and Timing Logic

This logic includes a crystal oscillator and various counters to produce:

1) A line scan RLSC0-3 ORed with RD1-4 to produce GLSC0-3.

2) Timing and clocks for the control logic (clock A, clock C, etc).

3) 13 baud rate clocks of which eight will be used by the AMLC in any one configuration.

f) Line Interface Logic

This logic consists of 16 UARTs and associated logic to enable transmission of mark or space characters, select one of eight clocks, and loop the transmit data to the receive input. Also included are one data set control bit and one data set sense bit per line.

g) Control Logic

This logic takes the outputs of the UART Status Register and the control bits from RAMC and decides what action to take, i.e., DMT request for next transmit character, DMT input to clear CPU dedicated cell is a valid character received from CPU, or DMA/DMC input to CPU with a received character or line status condition. This logic also writes new configuration and line control words when the I/O flag (FIOBY) is set.

h) UART Status Register

This is a 6-bit register used to hold UART status for use by the control logic. Bits stored are: Receive Data Available; Receive Data Parity Error; Receive Data Framing Error, Overrun Flag; Transmit Buffer Empty.

i) Received Data Register

Used to store Received Data from UART.

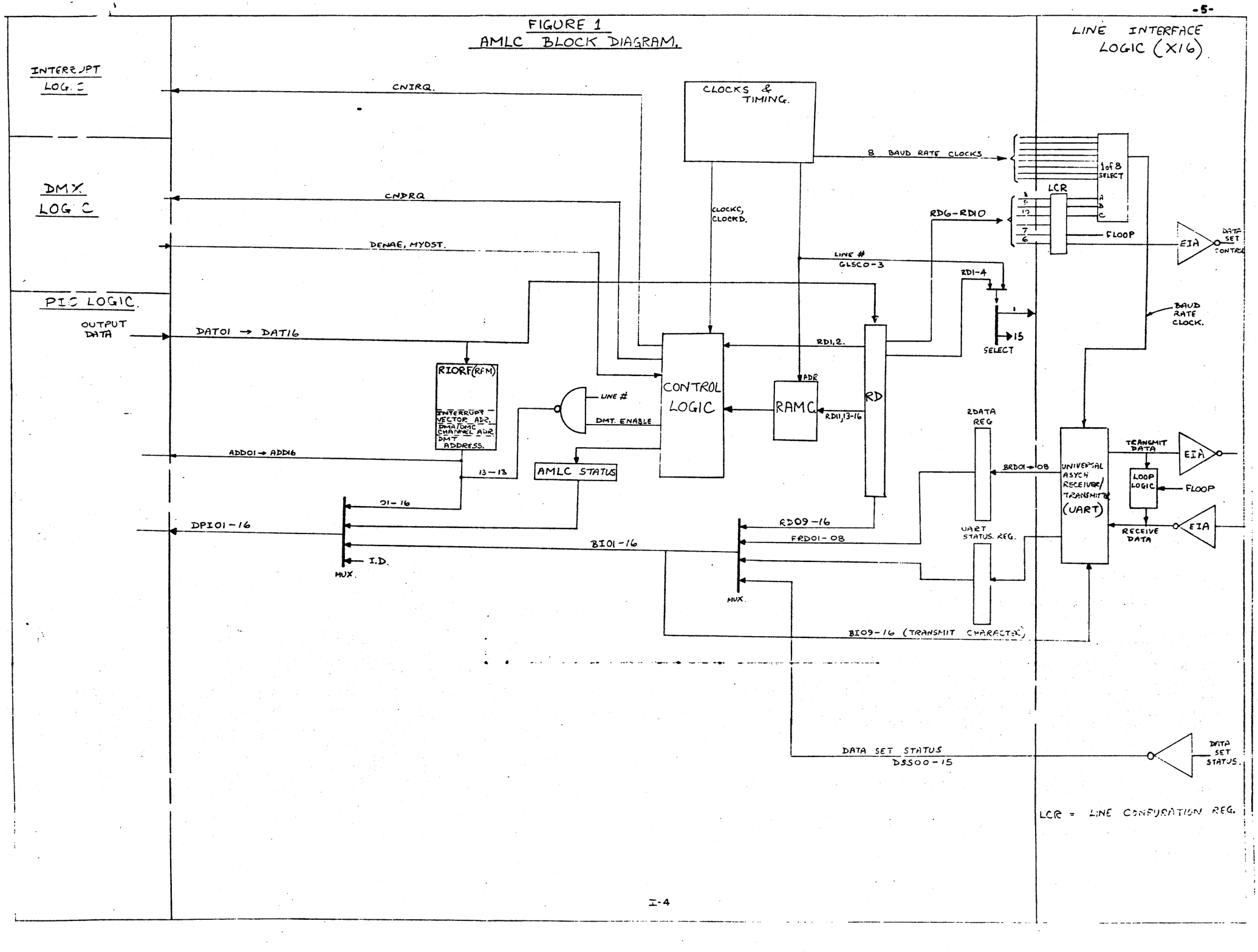
4. SOFTWARE INTERFACE

4.1 Programmed I/O

The Programmed I/O (PIO) instructions for the AMLC cause specific actions in the AMLC. The defined PIO instruction set for the AMLC is shown in Table 5.1.

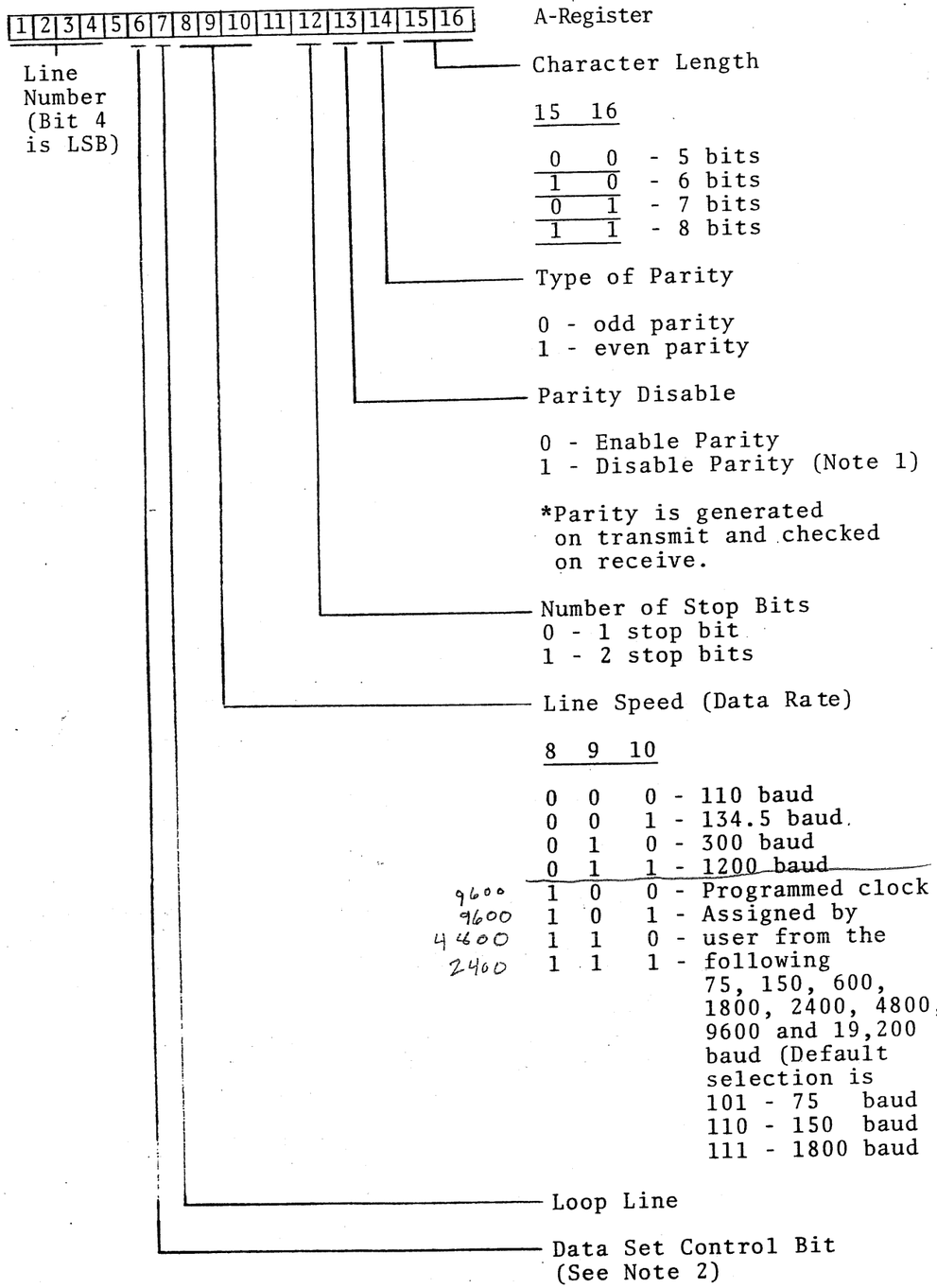
The standard device address for the AMLC is 54_8. This can be changed by means of jumpers.

FIGURE 1
AMLC BLOCK DIAGRAM.



a) Output Line Configuration

OTA '0154

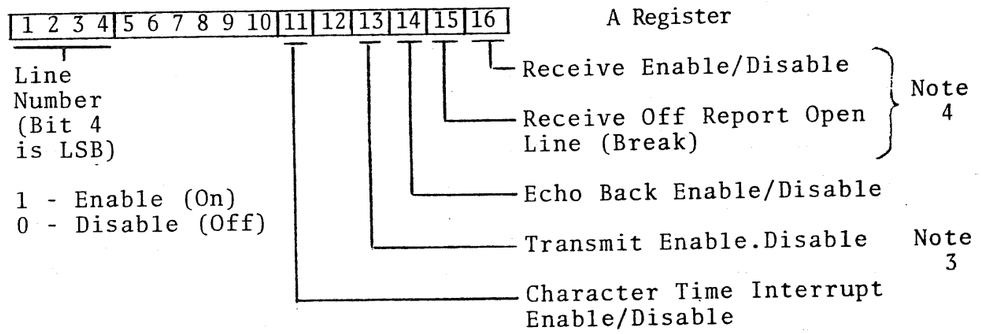


Note 1 - The parity bit if enabled is additional to the character bits. (i.e. It is concatinated with the character. It is last bit to be transmitted.)

Note 2 - On the basic AMLC board there is provided one control lead per line. Typically this could be used as "Request to Send" or "Data Terminal Ready" where some partial subset of full data set control is sufficient for customers uses. (Models 5052, 5054 only.)

b) Output Line Control

OTA '0254



Note 3 - Transmit and/or character time interrupts should not be enabled when echo back is enabled.

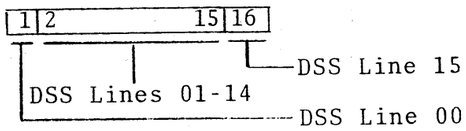
Note 4 - Bits 15 & 16 should never both be set at any one time.

c) (i) Models 5052, 5054

Input Data Set Sense (or status) Bit (DSS)

Typically this bit will be used for 'Clear to Send' when connected to modems or peripherals with a serial EIA interface. Data sense in the A-Reg is: 1 → Off, 0 → On.

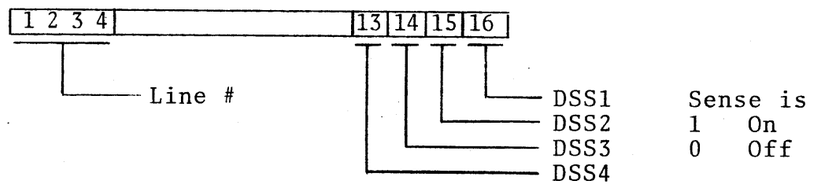
INA '0054



(ii) Models 5002, 5004

INA '0054 (Changed Format from Model 5052, 5054)

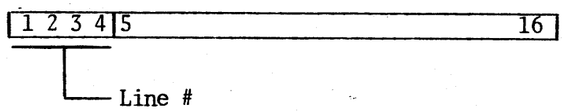
Input Data Set Status and Line #. This instruction should follow an OTA '0054.



A Register Bit	SIGNAL/TYPE OF MODEM			
	103A	103F	202 C/D	113
16	Clear to Send	Clear to Send	Clear to Send	Clear to Send
15	Data Set Ready	Data Set Ready	Data Set Ready	Data Set Ready
14	Carrier Detect	Carrier Detect	Carrier Detect	Carrier Detect
13			Supervisory Received Data	

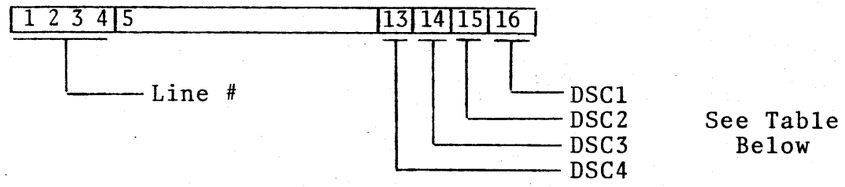
d) OTA '0054 (Model 5002, 5004 only)

Output Line # to Read Data Set Status. This instruction should be followed immediately by INA '0054 (see below).



e) OTA '0354 (Model 5002, 5004 only)

Output Data Set Control



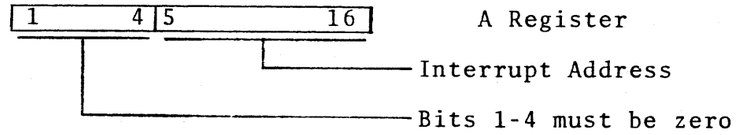
A Register Bit	SIGNAL/TYPE OF MODEM			
	103A	103F	202 C/D	113
16		Request to Send	Request to Send	
15	Data Terminal Ready		Data Terminal Ready	Data Terminal Ready
14		Originate Mode	Supervisory Transmit Data	
13		(Note 1) Local Mode		Terminal Busy

Note 1 - Control of the 'Local Mode' lead on a type 103F modem can only be achieved by changing jumpers on the DSC board. See diagram below.

There are 4 jumper DIP sites on the DSC at locations 6L, 14L, 29M and 43L. The jumper DIPs are set up as shown below.

f) Output Interrupt Vector Address

OTA '1654



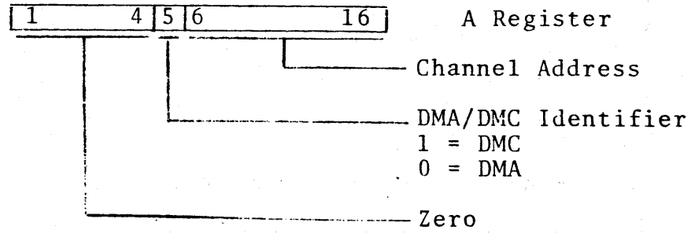
g) Input Interrupt Vector Address

INA '1654

A-register contents should be identical to that shown for OTA '1654 (Output Interrupt Vector Address).

h) Output DMA/DMC Channel Number

OTA '1454



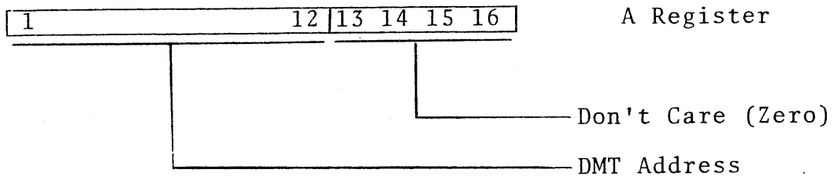
j) Input DMA/DMC Channel Number

INA '1454

A-register contents should be identical to that shown for OTA '1454.

k) Output DMT Base Address (Bits 1 through 16)

OTA '1554



Note: Due to the way DMT is used, no End Address is necessary. For further details see data transfers AMLC ↔ CPU (Transmit). Address Bits 00 and 99 will always be zero.

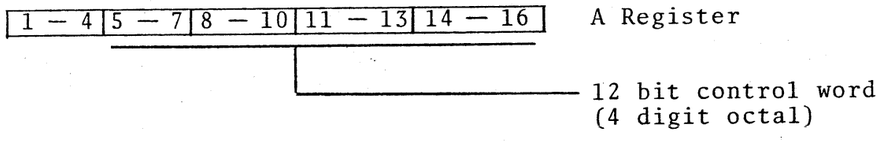
l) Input DMT Base Address (Bits 1 through 16)

INA '1554

A-register contents should be identical to that shown for OTA '1554.

m) Output Programmable Asynch Clock Control Constant

OTA '1754



A 12 bit word is loaded into the A-register bits 5 through 16 and is output to a register on the AMLC which controls a 12 bit counter. Below is a table of constants to be loaded to generate certain specific data baud rates.

The formula for calculating clock constants is:

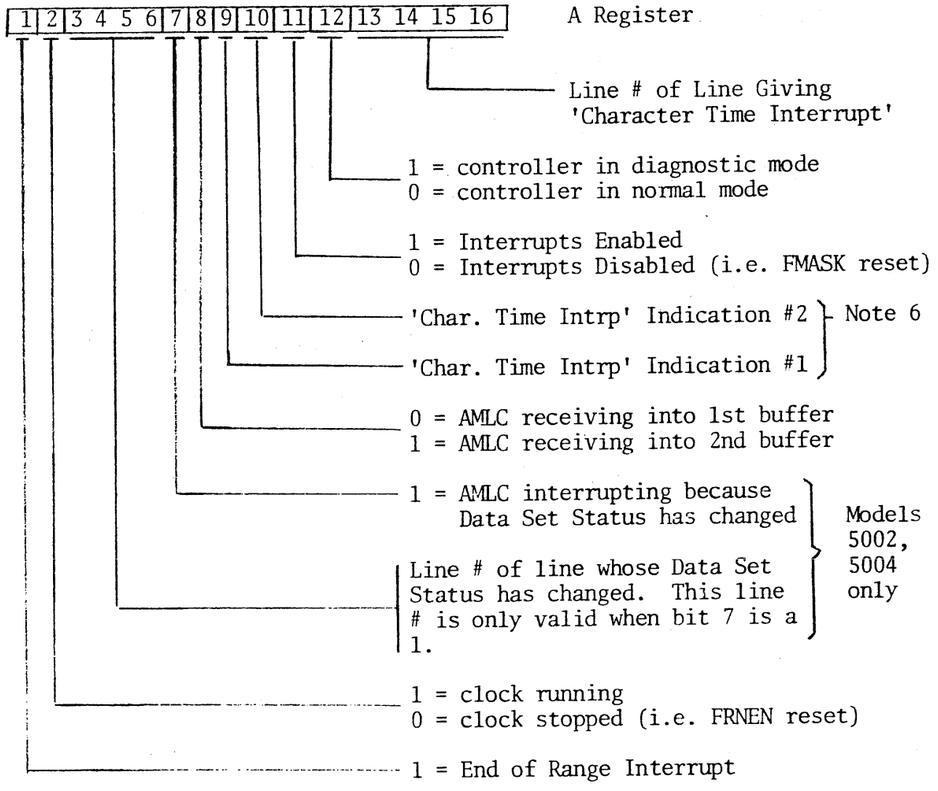
$$(\text{A Reg})_{10} = \left(\frac{115200}{fc}\right) - 1$$

when fe = baud rate

Baud Rate Required	Constant 8	Actual Baud Rate
30	6557	30.001
45	4777	45.002
50	4377	50.002
55	4056	54.991
100	2177	100.005

n) Input AMLC Status (and Clear) (This instruction will always skip.)

INA '0754



Note 5 - When INA '0754 is performed, bits 9, 10, 3-7 and 13-16 are cleared to zero.

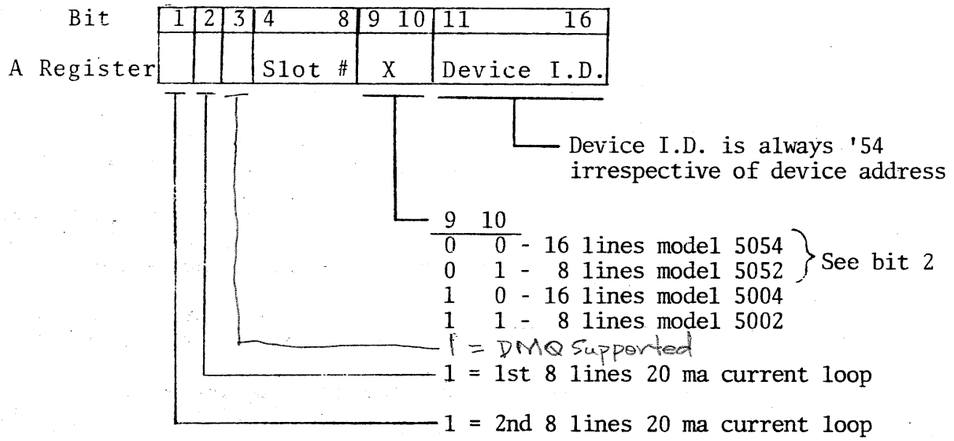
Note 6 - A character time interrupt will set bit 9 and put the line # on bits 13 through 16. If before an INA '0754 can be performed, a second character time interrupt occurs, bits 9 and 10 will both be set and a new line number will be set in bits 13 through 16.

To the programmer bits 9 and 10 both being set means that the line whose number is in bits 13 through 16 has interrupted and another line had previously interrupted but the line # has been overwritten.

o) Input AMLC I.D.

INA '1154

The format of the data in the INA I.D.



Where the Slot # is encoded as follows:

Name	Conn Pin	I/O Bus Bit
BMCEXS1	A-87	4
BMCEXS2	A-89	5
BMCSS01	A-91	6
BMCSS01	A-93	7
BMCSS03	A-95	8

The Slot # is encoded on the backplane and this information is simply "passed on" during the INA. The X is for variation of the basic device type called out in the I.D. and is normally 00.

The Device I.D. is the standard device address for that type of device, in this case 54_8, and is intended to identify the type of device that is in the system.

p) Skip if 'Not Interrupting'

SKS '0454

This SKS tests the AMLC Interrupt and will skip if the AMLC is not interrupting.

q) Initialize

OCP '1754

This command will clear all flip-flops and registers in the AMLC, start the AMLC clock and over a period of one line scan, clear all the line control bits in RAMC to zero. For the period of the one line scan the AMLC will respond not ready to PIO instructions.

r) Enable/Disable Interrupts

OCP '1554 Set Mask (Enable Interrupts)
OCP '1654 Reset Mask (Disable Interrupts)

s) Normal/Diagnostic Mode

OCP '1254 Set Normal Mode
OCP '1354 Set Diagnostic Mode

In normal mode it is possible to run all lines and issue all OTA, INA commands. In diagnostic mode, it is possible to do all the above plus OCP 'stop clock' and OCP 'single step clock' for debug purposes.

t) Stop Clock and Single Step Clock

OCP '0054 Stop Clock
OCP '0154 Single Step Clock

These two commands are specifically designed as debug aids and are only effective when the AMLC is in the diagnostic mode.

4.2 Data Interface

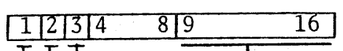
Data transfers CPU - AMLC are by DMA or DMC for 'Received Data' and 'Line Status' (i.e. frame error, break, etc.) and DMT for Transmit Data.

a) Transmit Data

A location in RIORF will store bits 1-12 of the DMT address and bits 00 and 99 will always be zero.

This 14 bit address will locate a CPU memory address the last four bits of address being zero. By concatenating the four bit line number with the stored 14 bit address and presenting the whole 18 bits on the address lines during DMT cycles the AMLC can access a block of 16 CPU memory cells anywhere in 64K of memory. These 16 cells will be referred to as dedicated cells.

When a DMT request is made the AMLC will fetch the contents of the dedicated cell (D.C.) and inspect bits 1, 2 and 3, the data format is shown below.



Data Format in D.C.

Control Bits (1, 2 and 3)

Bit 1, 1 = Valid Character in Bits 9-16
0 = No Character, Inspect Bit 2

Bit 2, 0 = Mark Line for a Character Time
1 = Space Line for a Character Time

Bit 3, Idle bit, used purely for software/AMLC coordinated timing purpose. See below.

Character (5, 6, 7 or 8 bits, LSB in bit 16)

The AMLC will input the DC to the RD register and will inspect bits 1, 2 and 3. If any of these bits is a 1 the AMLC requests another DMT cycle, but this time make an input with an all zero character to clear DC. The software knows when it sees DC cleared that data has been taken.

Within the AMLC bits 1 and 2 are always transferred with the character field to the line interface. Bit 3 is used as a timing device as follows:

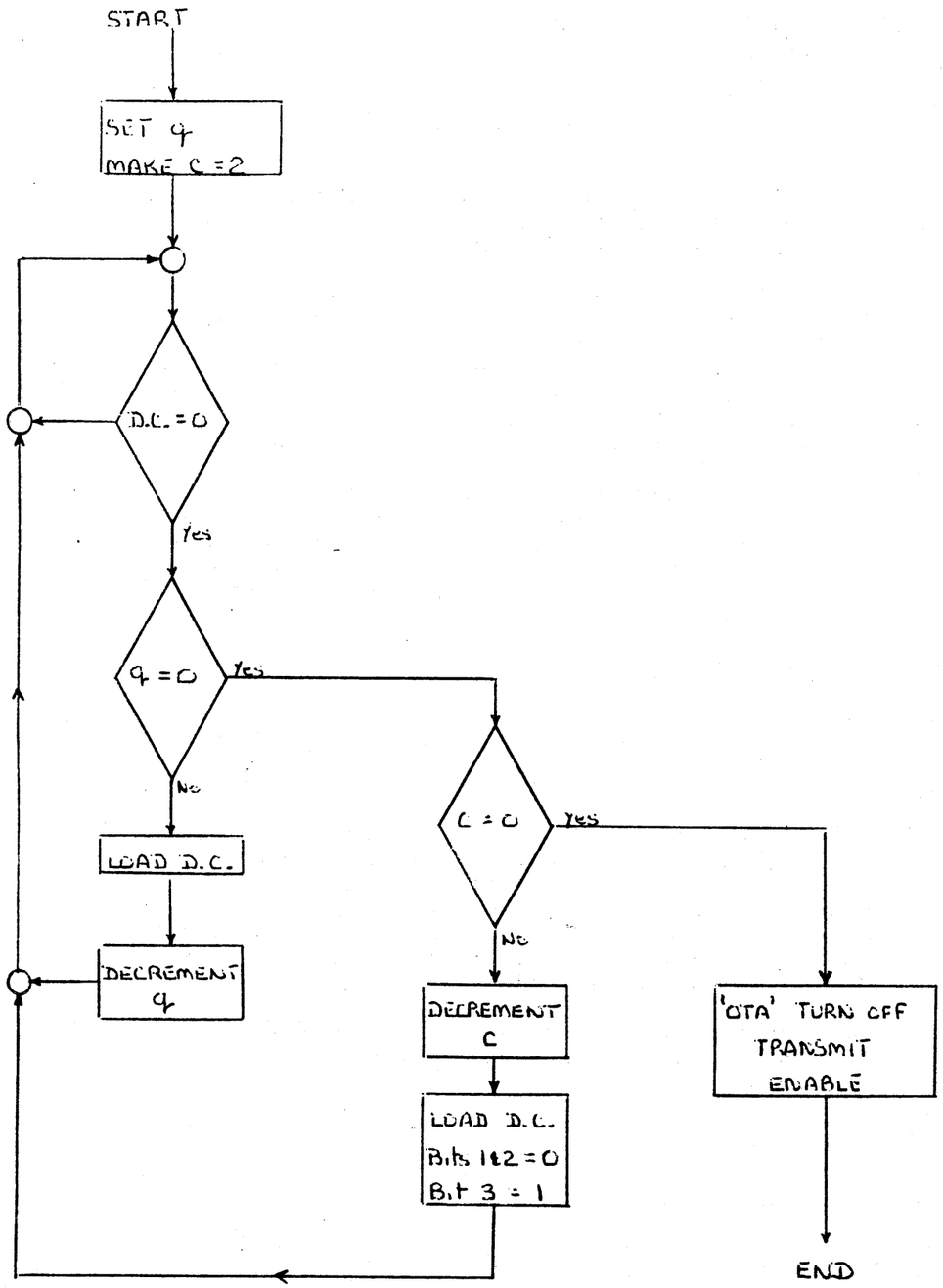
The use of UARTs in the line interface means that from the time the last character in a message is taken from the DC, approximately two character times will elapse before it is safe to disable transmit and enable receive. Let us assume that the software will maintain a queue (q) to indicate the number of characters left in a message and provide two bits per line as a two bit counter (C). To turn a line off at the end of a message bit 3 is set each time the DC is filled and used as an indication to software that the DC has been fetched by the AMLC. Bits 1 and 2 being zero means the line will start to mark at the conclusion of the message. The flow chart on the next page will explain the sequence of events to be followed.

b) Receive Data and Line Status

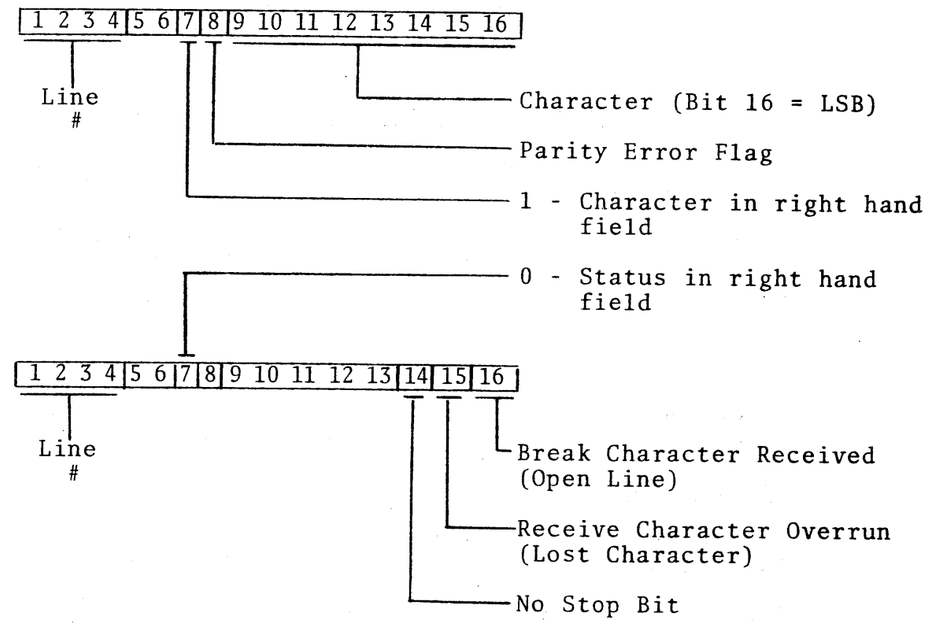
Received data and line status is inputted to the CPU via DMA or DMC. Input is to a tumble table, i.e. each input contains a line number and data (see below) and causes the DMA/DMC base address to increment.

Although only one DMA or DMC channel address is output to the AMLC (5.1.f OTA '1454), two adjacent channels will be used, i.e. two buffers in CPU memory. Bit 15 of the channel address is toggled by the AMLC every time an End of Range occurs. Thus, an End of Range will not cause loss of data if the software inputs AMLC status (INA '0754) within a buffer time.

Bit 8 of the AMLC status word will define which of the two input buffers the AMLC is currently using (see section 5.1.k).



Format for Received Data



4.3 Interrupts

a) End of Range (EOR)

The End of Range flip-flop (DEORF) is set by a signal from the CPU when one of the allocated DMA/DMC blocks of CPU memory has been filled. DEORF being set will cause the AMLC to change the channel address to the alternate buffer.

The interrupt routine should include an INA '0754 and the EOR will show up as bit 1 in the A-Register being set. INA '0754 will also clear the EOR.

b) Character Time Interrupts

Each line has a control bit enabling it to generate an interrupt every time the Transmit Buffer is empty. This interrupt will work regardless of the state of Transmit Enable, but should not be enabled when echo back is enabled.

When the software enters the AMLC interrupt routine it should perform an INA '0754. Bit 9 is the 'Character Time Interrupt' indication and bits 13-16 comprise the line number of the line causing the interrupt. The INA '0754 will reset bits 9 and 13-16 to zero.

This feature removes the need for a Real Time Clock option.

5. PIO Logic

5.1 The logic on LBD's 2-7 is standard to PRIME controllers. It incorporates PIO, DMX, Interrupt Logic and Data Bus.

The PRIME Peripheral I/O Bus is a high speed, bidirectional interface between the Central Processor (CP) and the various peripheral controllers. The bus is integral with the backplane and the AMLC plugs into this backplane. The device cables plug into the AMLC on the back edge connector and exit from the rear of the cabinet.

The I/O Bus transfers commands to the AMLC, data to or from the AMLC, status from the AMLC, and interrupts from the AMLC. These dialogues occur in one of several standard modes:

(1) Programmed I/O Mode

(2) Direct Memory Access (DMA) Mode

(3) Direct Memory Channel (DMC) Mode

(4) Direct Memory Transfer (DMT) Mode

(5) Interrupt Mode

The I/O bus consists of a subset of the signals on the backplane; 16 bidirectional data lines plus 2 parity lines, 18 bidirectional address lines plus 2 parity lines, and a number of unidirectional control lines. See Table 5-1 for a complete list of these signals.

The I/O bus is driven by a combination of control logic and μ-programmed routines in the central processor. The AMLC is either driven from the processor (in PIO mode) or bids for bus utilization (in all other modes). A determination of which device may utilize the bus is made by the processor based on which kind of utilization is requested and the physical location of the devices on the bus.

Parity - The AMLC will generate odd parity per byte on all input data transfers and check parity on all output data transfers (PIO and DMX). Address parity (odd per byte) will likewise be generated by the sender and checked by the sendee.

A parity error detected by AMLC on output (address or Data) will cause the AMLC to raise the appropriate Error Line on the I/O bus.

Mode Lines - The mode line encoding for all I/O operations is shown in Table 5-2. Note that all I/O operations require all five of these lines to be in the low impedance state (1 or 0).

5.2 I/O Bus Modes

5.2.1 Programmed I/O Mode (PIO)

In this mode, each data or control transfer on the bus is the direct result of the execution of a programmed input-output instruction in the central processor.

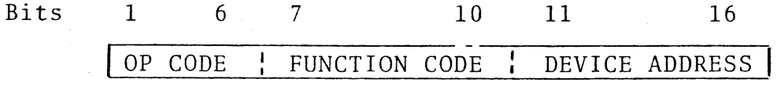
There are five such instructions on the AMLC:

Output Control Pulse (OCP)
Output from A Register (OTA)
Input to A Register (INA)
Skip if Ready Set (SKS)
Clear Active Interrupt (CAI)

These I/O instructions result in a single data or command transfer and/or a conditonal branch test in the central processor program. These instructions are described in detail in the text that follows. Note that all transfers that occur in this mode are directly controlled by the program currently being executed.

5.2.2 PIO Instruction Formats

OTA, INA, OCP, and SKS instructions have the instruction format shown below. The CAI instruction is a generic instruction.



This information is placed on the peripheral Address Bus during the execution of PIO commands.

Table 5-1

Input/Output Bidirectional Bus Signals

Pins	Direction	Name	Driver Type	Function
1	o	H SYS CLR-	TTL	System Clear
1	o	HPW RFL-	TTL	Power Failure Signal
1	o	BPC FCLK+	TTL	System Clock 5 MHz
1	o	BPC SCLK+	TTL	System Slow Clock 5/16 MHz
1	o	BPC STRB+	TTL	Strobe
5	o	BMC EXS1, 2- BMC SS01 thru 3-	OC	Slot Select
16	b	BPD01 thru 16+		Data
2	b	BPDLP, RP+	T	Data Parity
2	i	BPDPER-, L-	TTL	Data Parity Error
18	b	BPA 00+ thru 16+	T	Address
2	b	BPALP, RP+	T	Address Parity
2	i	BPAPER-, L-	TTL	Address Parity Error
1	i	BPC DRQ-	OC	DMA/DMC/DMT Request
1	o	BPC DEN+	T	DMA/DMC/DMT Enable
1	o	BPC DCPN+	T	DMA/DMC/DMT Clear PriNet
5	i	BPC MODO+ thru 3+ BPC INMD+	T	Transfer Mode Encode
9	o	BPC DPNO- BPC DPNA thru H-	TTL	DMA/DMC/DMT PriNet
1	o	BPCEOR+	T	End of Block DMA/DMC
1	o	BPC PIO+	TTL	Programmed I/O
1	i	BPC REDY-	T	PIO Ready
1	i	BPC IRQ-	OC	Interrupt Request
1	o	BPC IEN+	T	Interrupt Enable

Table 5-1 (continued)

Pins	Direction	Name	Driver Type	Function
1	o	BPC ICPN+	T	Interrupt PriNet Clear
5	o	BPC IPNO- BPC IPNA thru D-	TTL	Interrupt PriNet
1	i	BPC IOVI-	OC	Interrupt Override Inhibit
1	o	BPC CHI+	T	Clear Highest Interrupt

OC = Open Collector T = Tri State TTL = T^2L

Table 5-2

PRIME 200 I/O Bus
Mode Line States

Mode Line Name	I/O Modes DMA	DMT	DMC	Special (Escape)	Programmed I/O	Interrupt
BPCMODO+	0	1	1	0	0	0
BPCMOD1+	1	0	1	0	0	0
BPCMOD2+	0	0	0	0	During INA 1=Clear A Reg. before INA 0=Logically OR A Reg Data Eise TBS	1=Memory Increment 0=Interrupt
BPCMOD3+	0	0	0	0	0	0
BPCINMOD+	1=Input 0=Output	1=Input 0=Output	1=Input 0=Output			

The OP Codes are:

COMMAND	OP CODE
OTA	74_8
INA	54_8
OCP	14_8
SKS	34_8

The function codes are used to further specify the type of command. Certain function codes have been assigned for the AMLC. This assignment is shown in Table 5-2.

The device addresses specify which controller is to respond to the command. In any given system there must never be two controllers with the same device address. The device address is preassigned as 54 and additional AMLC should have their device addresses changed.

On LBD 8 in the top left hand corner are shown two Header Dips. The device address can be changed by means of jumpers on these two dips located at sites 20E and 22E on the AMLC board.

A Device Identification Number is assigned to each type of device. It denotes the class of device as reflected by its instruction set. That is, if there are three AMLCs in a system, the three will have three different device addresses but the same I.D.; thus, if software were to issue an INA I.D. Number for all possible device addresses (0 thru 77_8) it would have compiled a list of all of the types of devices currently connected to the system.

The I.D. Number of any given device type is the standard device address for that device in bits 11 through 16 and a 00 in bits 9 and 10. Bits 9 and 10 will be non-zero where special versions (with different instruction set) must be visible to the system software.

5.3 DMX Logic

The DMX logic is shown on LBD.7.

The DMX fabric is constructed from four materials: (a) the controller DMX logic; (b) the I/O bus signals; (c) the central processor logic; and (d) the DMX u-code.

The DMX u-code and the central processor logic are defined for the current machine, but will in all likelihood change from model to model of the PRIME family of processors. The I/O bus and the controller logic is meant to remain invariant through the product life, so that controllers which run on the PRIME 215 will run on any machine in the family.

The DMX I/O bus interface logic is standard in every controller (if the controller utilizes the DMX). The controller DMX logic connection to the I/O bus consists of the following signals:

DMX Enable - output
DMX Clear Priority Net - (9) 1 output; 8 input
DMX End of Range - output
Strobe - output
DMX Request - input
Address and Address Parity - (20) bidirectional
Data and Data Parity - (18) bidirectional
Data Parity Error - (2) input
Mode Lines - (5) input

The controller DMX channel number is typically loaded into the controller by a programmed I/O (PIO) instruction. The controller is then enabled in the DMX transfer mode (input, output, DMA, etc.) and started by the same or another PIO instruction. When the controller is ready to make a transfer (typically device determined), it activates the DMX request line, driving the open collector output to ground (see Figure).

The processor (CP), when it senses that some device has driven the DMX request line to ground, traps to the DMX u-code. A DMX Enable pulse is then sent to all controllers. The leading edge of this pulse staticizes each controller's DMX request in the DPNRQ flip-flop. This staticized line goes to the priority network. Thus any controller which had its DMX request line active when the leading edge of DMX Enable is received gets its request into the priority network, is not considered for this cycle, and must wait for the next DMX Enable pulse to be considered again.

The priority network takes the staticized request lines and determines which controller is the highest priority requesting controller.

This network has look-ahead logic in it to speed up the priority determination. The network begins to stabilize at the leading edge of the DMX enable signal, when its inputs are staticized. The network takes a defined amount of time to stabilize (approximately 160 nanoseconds). At this time the priority net in the controller will either be a zero - implying that the controller is not the highest priority requesting controller, and; therefore, DMX operations which will follow are not to affect that controller; or a one - implying that if the staticized request line is high then that is the highest priority requesting controller, and the subsequent DMX cycle is for it. This begins the address phase of the cycle. The trailing edge of the DMX Enable pulse is used to staticize this condition in the controller by setting a flip-flop (DENAL). Thus, the width of the DMX Enable pulse is determined by the time it takes for the DMX priority network to settle (predefined for all PRIME machines).

The DENAL flip-flop being set causes the controller to enable all of the tri-state address drivers putting the DMX channel number on the I/O bus address lines. At the same time all of the mode line tri-state drivers are enabled putting mode information (input/output, DMA/C/T, etc.) on the I/O bus mode lines. These lines are left enabled until the controller receives the leading edge of the next DMX Enable pulse which terminates the address phase of the transfer. Note that controllers must have address and mode information stable and meaningful at the inputs to the tri-state drivers for the duration of the time that the drivers are enabled.

Some time between the DMX Enable pulses the processor will generate a pulse called DMX Clear Priority Net. The leading edge of this pulse clears the staticized request signal that is the controller's input to the priority network (DPNRQ). Note that this flip-flop is cleared in all controllers at this time, not just the controller receiving the cycle. The signal also jams the priority network output from the controller to the high state (not requesting) for the duration of the signal. This forces the look-ahead logic in the priority network to the cleared state thus achieving a very fast clearing of the entire priority net.

The trailing edge of the Clear Priority Network signal clocks the current state of the DMX End of Range Line into the DEORF flip-flop.

The data phase of DMX cycle is initiated by the leading edge of the Strobe. This will set the DENDL flip-flop in the highest priority requesting controller. This in turn enables the tri-state data drivers if the controller is in the input mode. These drivers will be enabled for the duration of the Strobe in the input mode. The data at the input to the drivers must also remain stable and meaningful during this time.

The trailing edge of the Strobe will clear the DENAL flip-flop and must also be used to clock output data into the holding register. Output data cannot be depended on at the leading edge or during the Strobe.

The trailing edge of the Strobe terminates the data phase of the transfer.

The End of Range Line will be valid during the trailing edge of the DMX Clear Priority Net Signal. This line is staticized in the DEORF flip-flop and must be used to inhibit further controller requests if transfers are to cease.

This flip-flop must be cleared by the controller when appropriate to the controller's operation.

Some controllers may scatter and gather data in memory and may get several end of ranges before terminating the transfer. The disk controller does this by executing successive transfers on sequential DMA channels. So the End of Range signal is not necessarily used to terminate the transfers.

The implementation chosen for the DMX logic in the controllers imposes a few additional constraints on the DMX operation. These are:

a) The controller request signal (internal to the controller) once activated must remain high until it is cleared by the DENAE signal which is generated specifically for this purpose.

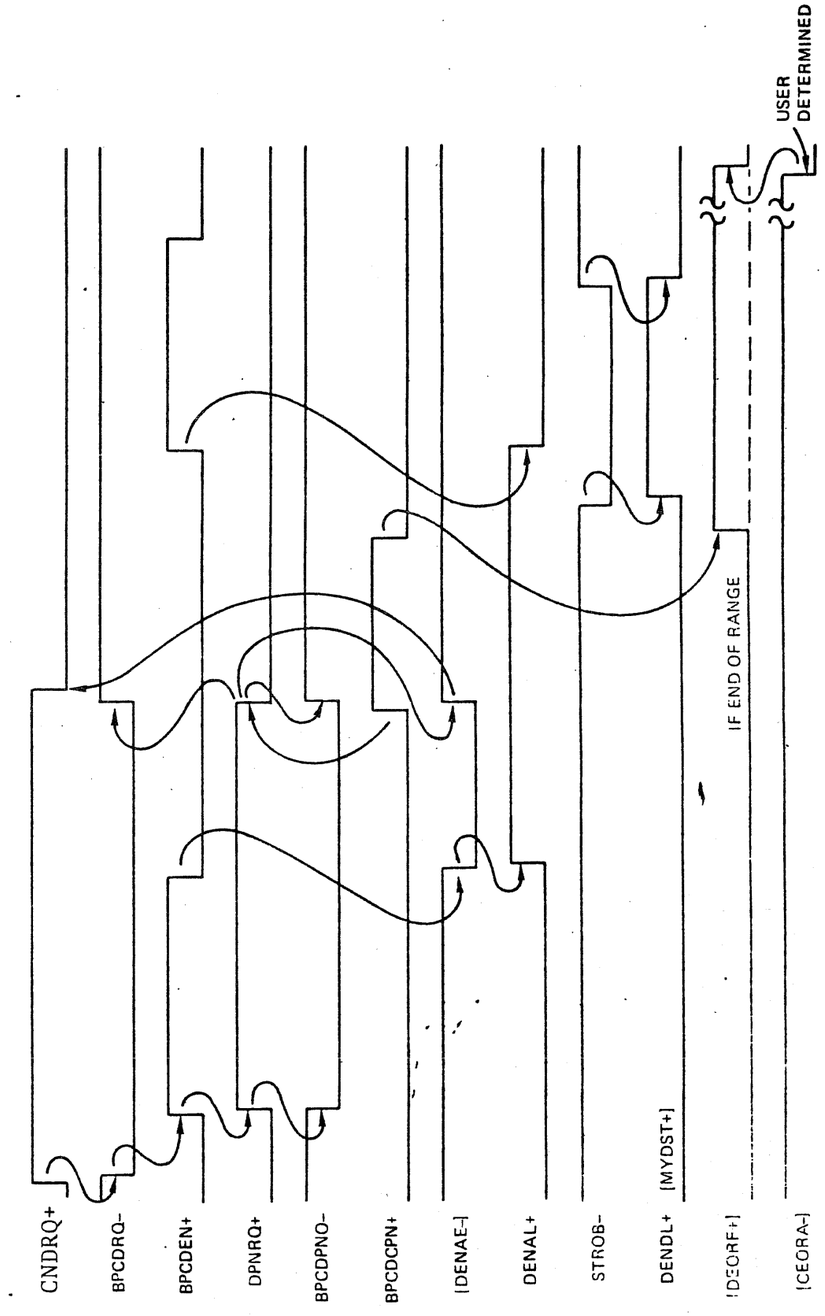


Figure 5-1. DMx Timing Relationships

b) The DMX Request signal (on the I/O bus) must only be gated onto the bus during the DMX Enable if its request has been staticized in the DPNRQ flip-flop. When DMX Enable is low any request may be placed on the I/O bus.

c) The Clear Pri Net signal must fall between the trailing edge of the previous DMX Enable and the leading edge of the next DMX Enable.

d) The data phase (i.e., the leading edge of Strobe) must begin prior to the end of the address phase (i.e., the leading edge of the next DMX Enable).

e) In order to allow successive transfers to occur as rapidly as possible, the u-code (in the PRIME 200) will always issue another Enable pulse and one more Clear Pri Net signal, following a successful transfer. This is not required by the hardware. But the hardware is designed to not care. That is, if a DMX request has been staticized by the leading edge of this "last" Enable Pulse, the processor will see only that (those) requests on the Request line while Enable is true. If no request had been staticized by the "last" enable the "last" DMX cycle must be aborted and a new cycle started (starting with another Enable Pulse) when the DMX request line causes the u-code to branch.

Timing

The detailed calculations of the various constraints on the I/O bus timing are available for completeness, but are not included here. The results of these calculations are shown in Figure 5-1. These are worst case numbers for the current design.

5.4 Interrupt Logic (LBD.6)

As in the case of the DMX, the Interrupts are comprised of (a) the Controller logic, (b) the I/O bus signals, (c) the central processor logic, and (d) the u-code.

Interrupt u-code and CP logic will in all likelihood differ for the various models of the PRIME family. The controller interrupt logic and the I/O bus are intended to be the same for all members of the product line. This insures that current controllers will run on all versions of the machine.

The Interrupt interface logic in the controller is standard for all controllers. This controller logic is shown in Appendix A for design purposes. There are actually three interface designs: one is the Interrupt Logic with Override Inhibit Interrupts; the second is the Interrupt Logic without Override Inhibit Interrupts; and the third is the Interrupt Logic with only the Override Inhibit Interrupt.

The connection to the I/O Bus consists of the following signals:

Interrupt Enable - output
Interrupt Clear Priority Net - 1 output, 4 input
Normal Interrupt Request - input
Override Inhibit Interrupt Request - input
Address and Address Parity - 20 input
Clear Highest Interrupt - output
Mode Lines - 5 input

The interrupt vector (if used) is generally loaded into the controller by a programmed I/O instruction. This address is then placed on the address bus during the address phase of the interrupt. The current implementation of controllers allows up to a 12 bit address to be specified. This address will not be used during compatible Mode Interrupts

When the controller is ready to request a Normal Interrupt (typically device determined) the controller activates the interrupt request line, driving the open collector driver to ground. If an Override Inhibit Interrupt is required, the Override Inhibit line is also driven to ground.

The processor (CP), when it senses that some device has driven the Normal Interrupt Request Line to ground, traps to the Interrupt u-code. An Interrupt Enable pulse is then sent to all controllers. The leading edge of this pulse staticizes each controller's Interrupt request in the IPNRQ flip-flop. This staticized line goes to the priority network. Thus any controller which had its Interrupt Request line active when the leading edge of Interrupt Enable is received gets its request into the priority network. If a controller's request line is activated after the leading edge of Interrupt Enable, it does not get into the priority network, is not considered for this cycle, and must wait for the next Interrupt Enable pulse to be considered again.

The priority network takes the staticized request lines and determines which controller is the highest priority requesting controller.

This network has look-ahead logic in it to speed up the priority determination. The network begins to stabilize at the leading edge of the Interrupt enable signal, when its inputs are staticized. The network takes a defined amount of time to stabilize (approximately TBS nanoseconds). At this time the priority net in the controller will either be a zero - implying that the controller is not the highest priority requesting controller, and; therefore, Interrupt operations which will follow are not to affect that controller; or a one - implying that if the staticized request line is high then that is the highest priority requesting controller, and the subsequent Interrupt cycle is for it. This begins the address phase of the cycle. The trailing edge of the Interrupt Enable pulse is used to staticize this condition in the controller by setting a flip-flop (IENAL). Thus, the width of the Interrupt Enable pulse is determined by the time it takes for the Interrupt priority network to settle (pre-defined for all PRIME machines).

The IENAL flip-flop being set causes the controller to enable all of the tri-state address drivers putting the Interrupt vector number on the I/O bus address lines. At the same time all of the mode line tri-state drivers are enabled putting mode information (Memory increment, etc.) on the I/O bus mode lines. These lines are left enabled until the controller receives the leading edge of the Interrupt Clear Priority Net pulse which terminates the address phase of the transfer. Note that controllers must have address and mode information stable and meaningful at the inputs to the tri-state drivers for the duration of the time that the drivers are enabled.

Some time between the Interrupt Enable pulses the processor will generate a pulse called Interrupt Clear Priority Net. The leading edge of this pulse clears the staticized request signal that is the controller's input to the priority network (IPNRQ). Note that this flip-flop is cleared in all controllers at this time, not just the controller receiving the cycle. This signal also jams the priority network output from the controller to the high state (not requesting) for the duration of the signal. This forces the look-ahead logic in the priority network to the cleared state thus achieving a very fast clearing of the entire priority net.

When the CP is in the Vector Mode, Normal Interrupt cycles cause lower priority interrupts to be inhibited until a CAI instruction is executed. This stack-like operation is implemented by the BPCCHI I/O Bus line (Clear Highest Interrupt line), the HPAIF flip-flop, and the Priority Net input.

If a Normal Interrupt cycle is for this controller, the LHPAI line goes high and on the trailing edge of IENAP, the HPAIF flip-flop gets set. The flop being set will cause the Priority Net output (BPCINO) to be low as long as no Override Inhibit Interrupt from any controller (ISHIC) occurs. Thus, an Override Inhibit Interrupt request will force the Highest Active Interrupt flip-flop (HPAIF) to temporarily relinquish control of the Priority Net.

The HPAIF flip-flop will be cleared if the priority net indicates that this controller is the highest priority requesting device (IPNOR is high) and a pulse occurs on the Clear Highest Interrupt Line. This pulse will be generated by the interrupt u-code when the machine is in the Compatible mode. Therefore, this controller will not hold onto the priority net, except during the actual interrupt cycle. In the Vector Mode, this pulse will be generated by the Clear Active Interrupt Instruction and not the u-code.

The I/O bus timing is shown in Figure 5-2.

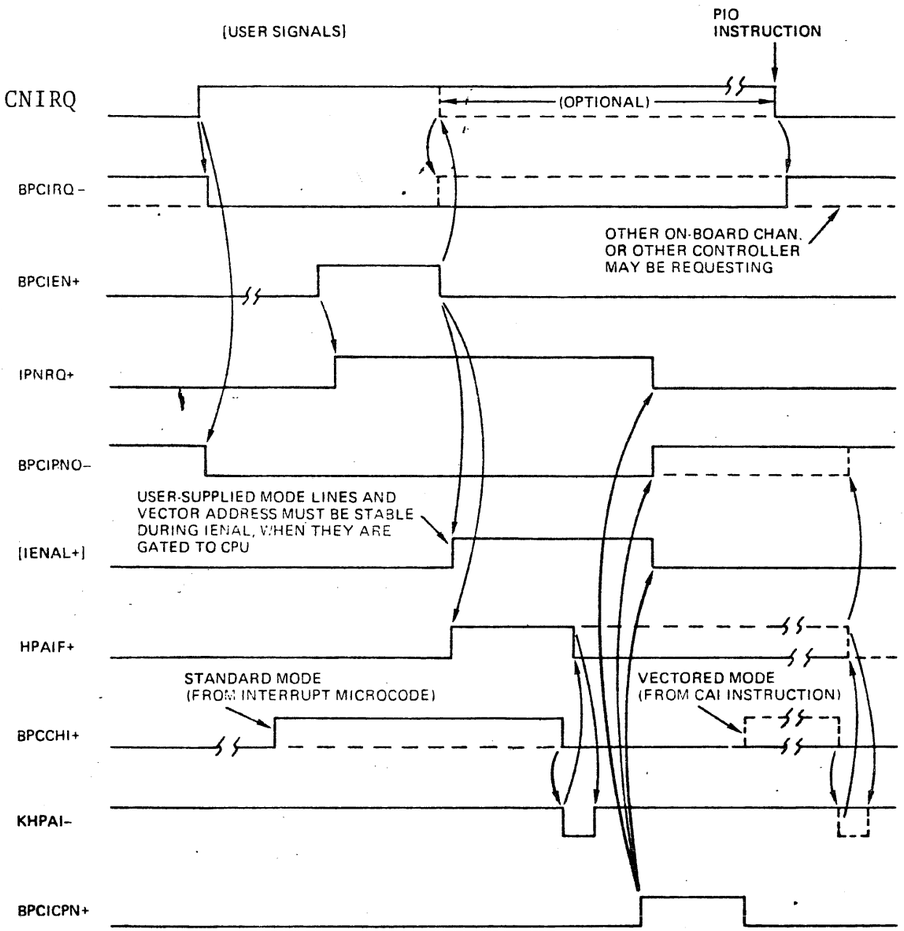


Figure 5-2. Interrupt Timing Relationships

TABLE 5.1 AMLC PIO INSTRUCTIONS.

OP CODE BITS 1-6 / FUNCTION CODE, BITS 7-10	14_8 OCP	34_8 SKS	54_8 INA	74_8 OTA
00	STOP CLOCK		INPUT DATA SET STATUS (DSS).	OUTPUT LINE# TO READ DSS. *
01	SINGLE STEP CLOCK			OUTPUT LINE CONFIGURATION.
02				OUTPUT LINE CONTROL.
03				OUTPUT DATA SET CONTROL. *
04		IF NOT INTERRUPTING.		
05				
06				
07			INPUT AMLC STATUS (& CLEAR).	
10				
11			INPUT I.D.	
12	SET NORMAL MODE.			
13	SET DIAGNOSTIC MODE.			
14			INPUT DMA/DMC CHANNEL ADDRESS	OUTPUT DMA/DMC CHANNEL ADDRESS.
15	SET INTERRUPT MASK.		INPUT DMT BASE ADDRESS (TX).	OUTPUT DMT BASE ADDRESS (TX)
16	CLEAR INTERRUPT MASK.		INPUT INTERRUPT VECTOR ADDRESS	OUTPUT INTERRUPT VECTOR ADDRESS.
17	INITIALIZE.			PROGRAMMABLE ASYNCH CLOCK.

* NOTE: MODELS 5002, 5004 ONLY.

6. AMLC LOGIC

6.1 Clocks and Timing

The clock and timing logic is shown on LBDs 11 and 12.

All AMLC timing is derived from a crystal oscillator 11/BO5 (i.e. LBD.11 grid reference BO5) or a series of OCP'0154s if in single step mode.

The crystal clock source is enabled by an OCP'1754 (Initialize) which sets FRNEN and FINIT.

CLKXX+ now causes counter at 11/K15 to count and clock pulses CLOCKA, B, C and D are produced. Some of these clocks are gated to produce CLSCAN- and CLWRM- (see figure 6.1).

CLSCAN- with CLOCKD+ increments the line scan counter RLSCO-3 (15/S05) and when all lines have been scanned once RLSCRY+ goes high and FINIT is reset.

While FINIT is set all locations in RAMC (14/TO5, 14/T10) are cleared. The write pulse EWRMC- is generated by FINIT- and CLWRM- (14/J12).

At 11/FO2, 11/K02, 11/P02 and 11/V02 is a counting chain which generates nine baud rate clocks of 19.2K, 9.6K, 4.8K, 2.4K, 1200, 600, 300, 150 and 75 baud for use by the "line interface logic". Baud rate clocks are clock signals at sixteen times the line baud rate (X16).

The counting chain at 11/KO5 and 11/PO5 produces the 1800 baud rate clock. That at 11/K08, 11/P08 and 11/V08 is for 110 baud, and that at 11/K12 and 11/P12 is for 134.5 baud.

On LBD.12 is the programmable clock logic. At 12/E03 and 12/E08 is the holding register for the constant output by the CPU with OTA'1754. This constant is loaded into counter at 12/K03, 12/K06 and 12/K10 to produce an output which is further divided by flip-flop CLAS04 12/R03. CLAS04 flip-flop is to guarantee a square wave pulse. For clock speeds close to maximum capabilities of UART in line interface we can now guarantee to minimum clock pulse width required.

6.2 Line Scan

At 15/S05 is the line scan counter. This counter is incremented by CLSCAN- when CLOCKD+ and SCINH- are high. (See Fig 6.1 for timing.)

The output of the line scan counter is gated at 15/W05 to become GLSCO-3. GLSCO-3 are decoded (13/D03) to give ERDOO-16. ERDXX- is the chip select for a specific line (1 of 16) and will enable the status outputs of the selected UART. These outputs and the outputs of the UART "Received Data Buffer" are staticized in registers (15/F02, 15/F04 and 15/F07) by CLWRM+ with CLOCKD- high.

If neither FRDAV or FTXBE are set the scan will increment with the next CLSCAN- with CLOCKD+ high.

If either FRDAV or FTXBE are set, SCINH- will go low (15/P01) and inhibit the line scan counter from incrementing. At 15/B11 SCINH- will cause SMICE+A to go high and if no PIO is in progress for the AMLC (DADOK - high) SMICE+ will be high and FMICRE (15/K09) will be set by the negative going edge of the next CLOCKC+.

FMICRE set will cause the "Common Control Logic" to write new "Line Control" or "Line Configuration" data
fetch a transmit character from the
CPU or transfer a receive character
(or/and status) to the CPU (see section 6.4). After the finish of these operations FMICRE is reset and the UART status register and receive register are cleared. This action will clear FRDAV and FIXBE, SCINH- will go high and the line scan can continue.

At the time that the UART status is stored in the UART status register, some of the register outputs and some of the outputs of RAMC are decoded by a PROM decoder (15/K04) to produce four control signals for the "Common Control Logic".

The 8 PROM inputs are FRDAV, FRDPE, FRDFE, FOVRN from the UART status register, GCHZR which is a decode (for an all zero character) of the received data register FRD01-08 and RRCEN, RRCOL, RECHM from RAMC. The 4 PROM outputs are GRCDMX, GSTDMX, GBRK and GECHM.

The flow chart in figure 6.2 shows the entire logic of the PROM decoder. The contents of the PROM are shown in table 6.1.

FIG 6.2

AMLC DECISION FLOW FOR STATUS-DECODE PROM (82526 @ Ø4F)

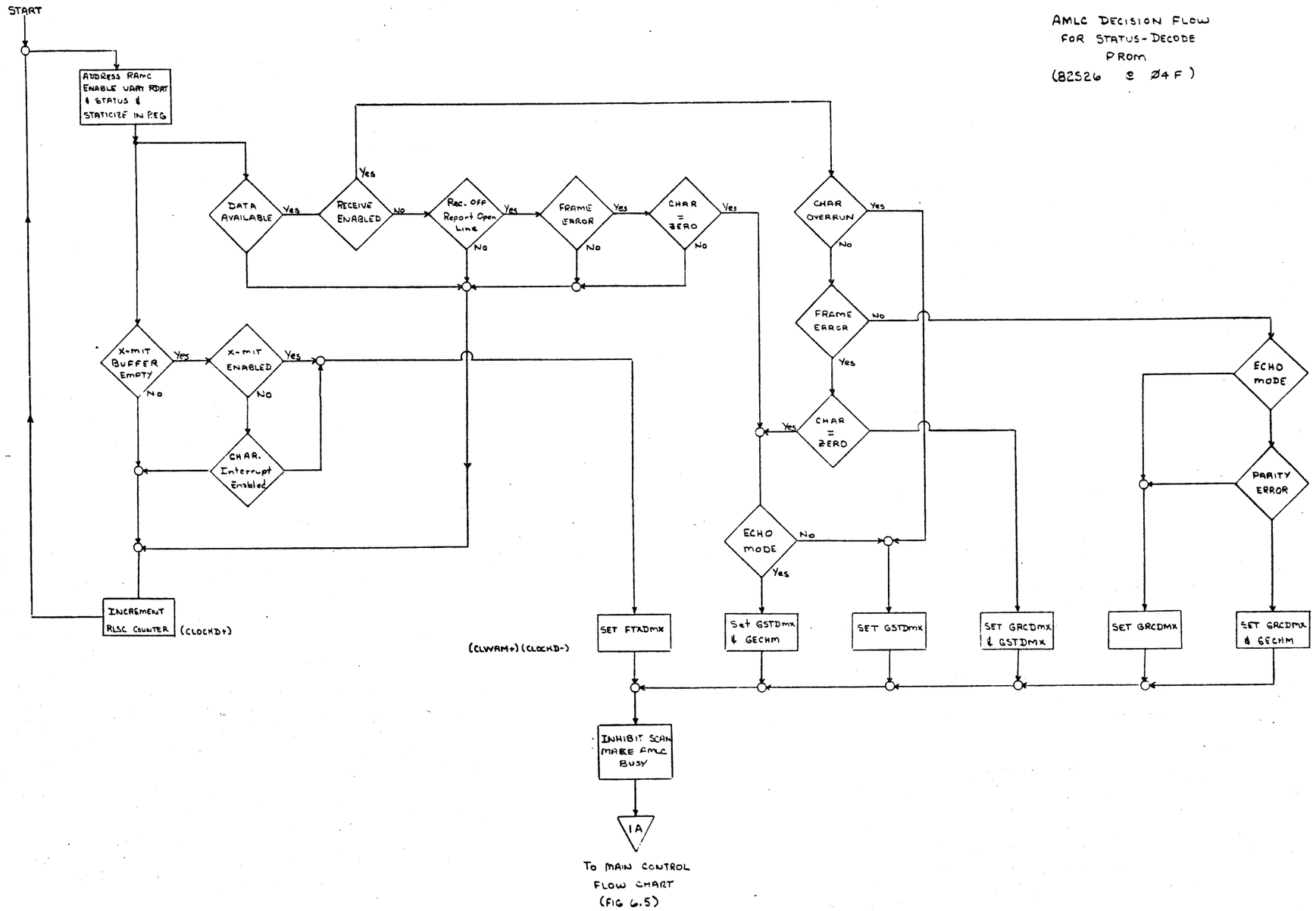


FIGURE 6.1. AMLC TIMING

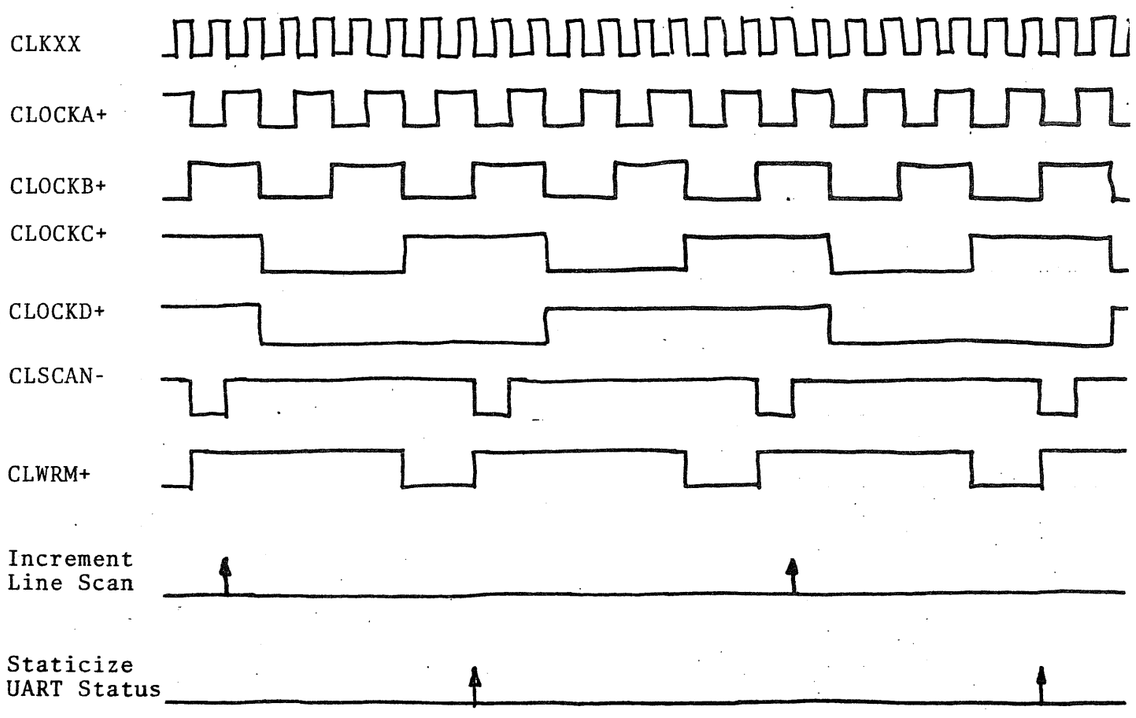


TABLE 6.1.

P-ROM CHART. for type 82S26 PROM in Dip Location 06(E,V) 04F(W,W (LBD 15/K04).

ADDRESS								OUTPUTS			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	04	03	02	01
1	0	0	0	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	0
1	0	0	0	1	0	1	0	1	0	0	1
1	0	0	0	1	0	1	1	1	0	0	1
1	0	0	1	1	0	0	0	0	1	0	0
1	0	0	1	1	0	0	1	0	1	0	0
1	0	0	1	1	0	1	0	0	1	0	0
1	0	0	1	1	0	1	1	0	1	0	0
1	0	1	0	0	1	0	0	0	1	1	0
1	0	1	0	0	1	0	1	0	0	0	0
1	0	1	0	0	1	1	0	0	1	1	1
1	0	1	0	0	1	1	1	0	0	0	0
1	0	1	0	1	0	0	0	0	1	1	0
1	0	1	0	1	0	0	1	1	1	0	0
1	0	1	0	1	0	1	0	0	1	1	1
1	0	1	0	1	0	1	1	1	1	0	0
1	0	1	1	1	0	0	0	0	1	0	0
1	0	1	1	1	0	0	1	0	1	0	0
1	0	1	1	1	0	1	0	0	1	0	0
1	0	1	1	1	0	1	1	0	1	0	0
1	1	0	0	1	0	0	0	1	0	0	0
1	1	0	0	1	0	0	1	1	0	0	0
1	1	0	0	1	0	1	0	1	0	0	0
1	1	0	0	1	0	1	1	1	0	0	0

GRCDMX+
GSTDMX+
GBRK+
GECHM+

ADDRESS								OUTPUTS			
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	04	03	02	01
1	1	0	1	1	0	0	0	0	1	0	0
1	1	0	1	1	0	0	1	0	1	0	0
1	1	0	1	1	0	1	0	0	1	0	0
1	1	0	1	1	0	1	1	0	1	0	0
1	1	1	0	0	1	0	0	0	1	1	0
1	1	1	0	0	1	0	1	0	0	0	0
1	1	1	0	0	1	1	0	0	1	1	1
1	1	1	0	0	1	1	1	0	0	0	0
1	1	1	0	1	0	0	0	0	1	1	0
1	1	1	0	1	0	0	1	1	1	0	0
1	1	1	0	1	0	1	0	0	1	1	1
1	1	1	0	1	0	1	1	0	1	0	0
1	1	1	1	1	0	0	0	0	1	0	0
1	1	1	1	1	0	0	1	0	1	0	0
1	1	1	1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	1	1	0	1	0	0

GCHZR-
RECHM+
RRCOL+
RRCEN+
FOVRN+
FRDFE+
FRDPE+
FRDAV+

NOTE

ALL OTHER PROM LOCATIONS CONTAIN ZERO.

6.3 Line Interface Logic (LIL)

This is the logic which is specific to each line and is shown on LBDs 19-26 (i.e. two lines per LBD).

The central part of the LIL is a UART (Universal Asynchronous Receiver/Transmitter).

The UART is a general purpose, programmable MOS/LSI device for interfacing an asynchronous serial data channel of a peripheral or terminal with parallel data of a computer or terminal. The transmitter section converts parallel data into a serial word which contains the data along with start, parity, and stop bits. The receiver section converts a serial word with start, data, parity and stop bits, into parallel data and it verifies proper code transmission by checking parity and receipt of a valid stop bit. Both the receiver and the transmitter are double buffered. The array is compatible with bipolar logic. The array may be programmed as follows: The word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhbited; the parity may be even or odd; and the number of stop bits may be either one or two.

Associated with each UART is a configuration register. This register holds a 3 bit address to select 1 of 8 baud rate clocks, a "data set control" bit and the "loop data" control bit.

This register and the "UART internal control registers" are loaded by a TCLSXX strobe from the "Common Control Logic".

6.3 (a) Transmit

Refer to figure 6.3. (Assume data stream shown is preceded and followed by valid character.) The UART is enabled by the line scan each time the line specific ERDXX signal is low. At this time the received data lines BRD01-08 and the UART status lines BOURN, BRDAV, BRDPE, BRDFE and BTXBE will be true.

If BTXBE is high the "Common Control Logic" will fetch a character from the CPU and output it to the UART with a TDLXX strobe. Along with the character are two control bits in RD1 and RD2. RD1 is gated to be GVCHR+ and RD2 is gated to be GMKSP+. If the GVCHR+ is high it means there was a valid character in the dedicated

cell in the CPU and FVCHXX will be set and the character will be loaded into the UART Transmit Buffer.

When the UART Transmit Register (parallel to serial) is empty and the stop bits or bit have been sent, the "Transmit Register Empty" signal TREXX+ will go high and the state of FVCHXX will be transferred to FTMDXX at the same time as the contents of the UART Transmit Buffer are transferred to the UART transmit register. With FVCAXX previously set and therefore FTMDXX now set, the output of the UART TDATXX+A will be outputted to the communications line as TDATXX+.

Now if RD1+ and therefore GVCHR+ had been low, FTMDXX would now be reset and the controlling factor for the transmit data stream will be the state of RD2 (GMKSP+) at the time that the UART was loaded by TDLXX. GMKSP controls FMSPXX and when TREXX goes high, the state off FMSPXX controls FMSPXX-A.

If RD2 was not set, TDATXX+ is an all mark character. If RD2 was set, then TDATXX+ is an all space character (break).

6.3. (b) Receive (See figure 6.4.)

The receive portion of the UART detects start, assembles a character, then transfers assembled characters to a receive buffer and sets "Receive Data Available" flag and other status flags.

When the line scan causes ERDXX- to go low, "Receive Data Available" and other status flags are available as BRDAV, BRDFE, etc.

If BRDAV is high the "Common Control Logic" will service the UART, take the character and generate a "Reset Data Available" to reset BRDAV.

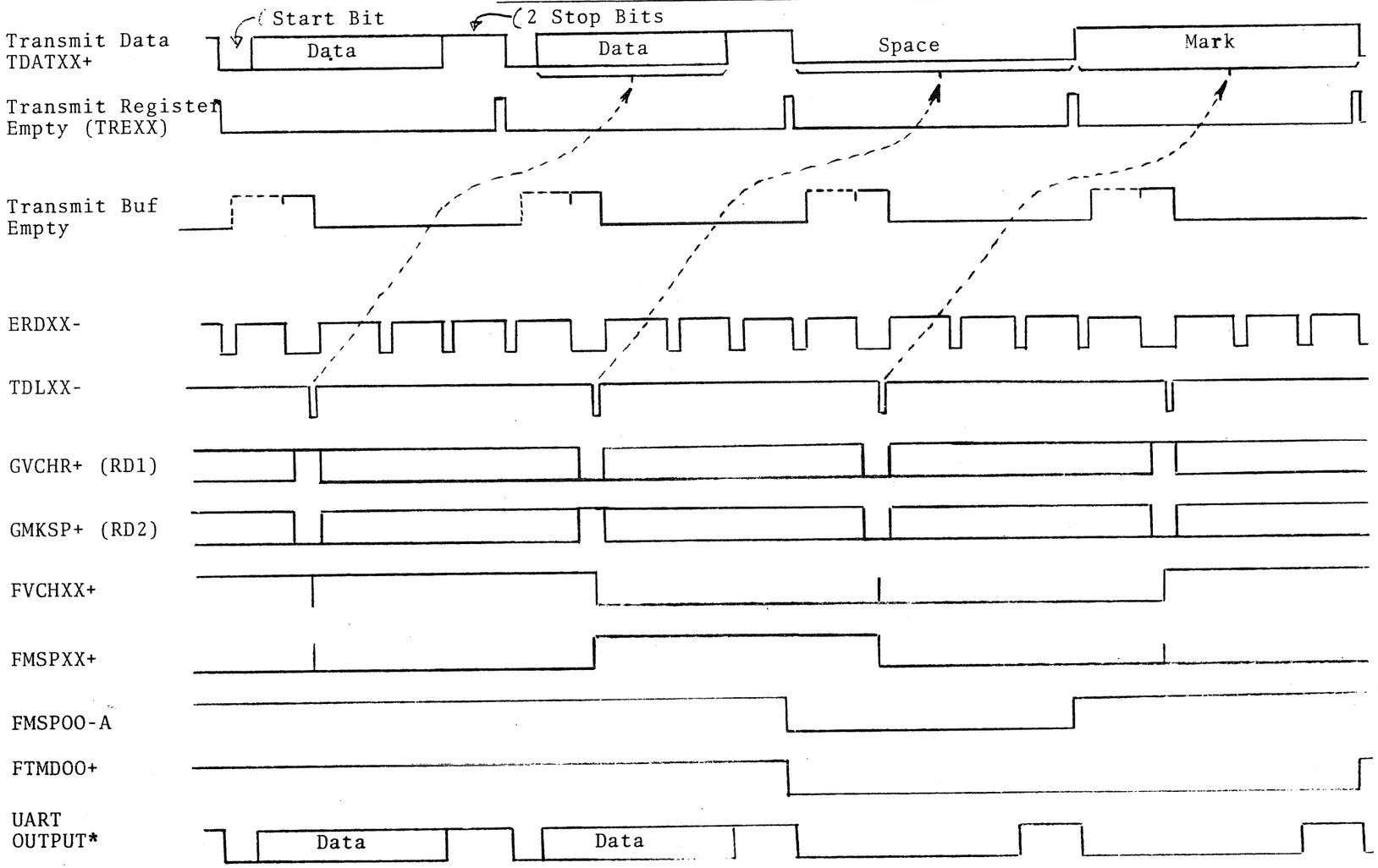
It should be noted that a "Break" is received as an "all zero character" and a "Framing Error" BRDFE.

An all mark character is not seen by the UART receive logic.

6.4 Common Control Logic

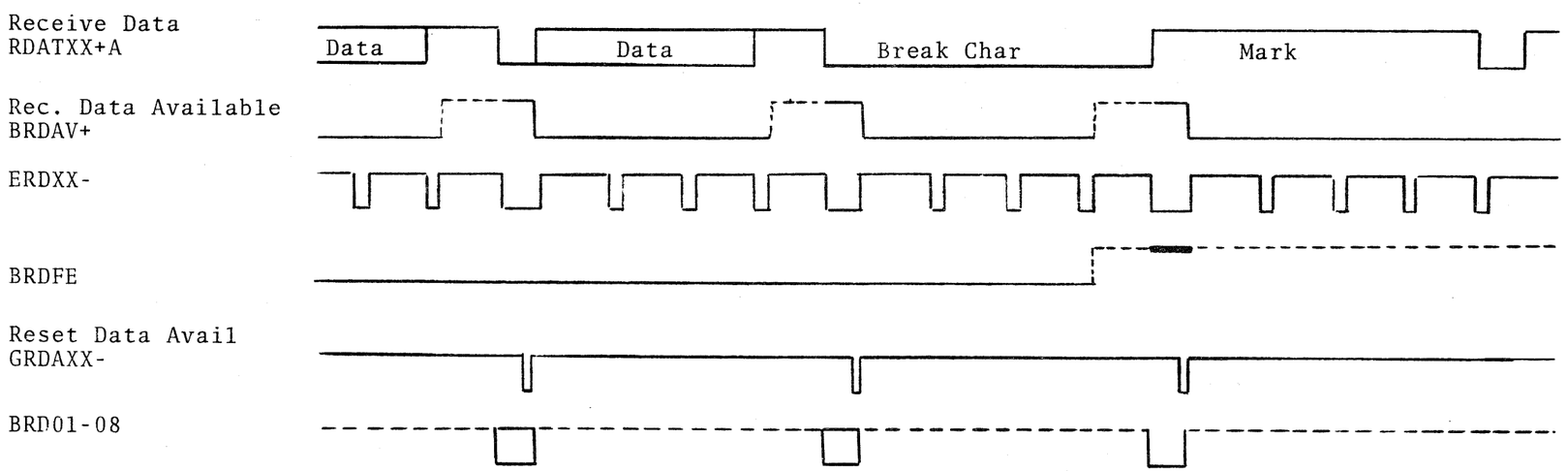
The "Common Control Logic" of the AMLC consists of PROM with a 24 bit wide word, a 24 bit register (RPM01-24) to hold the PROM outputs (PRM01-24), an

FIGURE 6.3. LINE INTERFACE LOGIC TIMING (TRANSMIT)



* Assume RD9-16 is zero if no valid character bit set.

FIGURE 6.4. LINE INTERFACE LOGIC TIMING (RECEIVE)



ALU and some decode logic.

The PROM address PRMAO-4 is derived from RPM bits 16-20. RPM16-20 go to an ALU which allows one of three conditions:

a) PRMAO-4 = (RPM16-20) + 1

This will increment address by 1.

b) PRMAO-4 = (RPM16-20) + 2

This will increment address by 2.

c) PRMAO-4 = (RPM16-20)

Address will be equal to RPM16-20.

The PROM is used primarily as a sequencer rather than a full u-program control.

The action of each bit in the PROM word is detailed in Table 6.2.

The Common Control Logic is used to:

a) Write "Line Control" information into RAMC, output Line Configuration data to Line Interface Logic, output Data Set Control data and staticize Data Set Status.

b) Fetch a Transmit Character from dedicated cell (see section 4.2. (a)) in CPU memory and clear cell if bits 1, 2 or 3 are set.

c) Transfer received data and/or status (break, overrun, etc) into a tumble table (see section 4.2. (b)) in CPU memory.

All these operations are covered by a flow chart (figure 6.5) and a table (table 6.3) showing contents of PRM01-24.

The only operation not covered by the flow charts is "End of Range" for Receive Buffer.

6.5 End of Range

As described in section 4.2. (b) two receive buffers are used with the AMLC. Which of the two channels is in use is controlled by FDMCHX (8/F13) which controls

TABLE 6.2. ACTION OF PRM01-24 IN COMMON CONTROL LOGIC

PRMXX	DESCRIPTION OF ACTION
01 08	1 | 8 0 | 0 - No Action 0 | 1 - Output A Strobe Pulse This pulse will write line control - RAMC, line configuration - line interface logic, [Data Set Control - Modem, or Staticize Data Set Status for Reading with INA'0054 (These last two on Models 5002, 5004 only)]. 1 | 0 - Transmit Data Load Strobe This pulse is steered by address in RD1-4 (GLSCO-3) to 1 of 16 UARTS, to output a "Transmit Character". 1 | 1 - Reset Receive Data Available This pulse is steered by address in RLSCO-3 (GLSC0-3) to 1 of 16 UARTS, to reset the receive buffer.
02 03	2 | 3 PRM02, 03 control the state or source for the two signals GVCHR, GMKSP. These two signals are outputted with a "Transmit Character" to cause output of a "Valid Character", "Mark Character" or a "Break". 0 | 0 0 -> GVCHR, 0 -> GMKSP (Output Mark) 0 | 1 0 -> GVCHR, 1 -> GMKSP (Output Break) 1 | 0 1 -> GVCHR, 0 -> GMKSP (Output Valid Character) 1 | 1 RD1 -> GVCHR, RD2 -> GMKSP
04	Make DMX request to CPU (CNDRQ+)
05 06	These two bits control the DMX mode. 5 | 6 0 | 0 - Not Effective 0 | 1 - DMT Output Mode [Input Data = 0 (Don't Care)] 1 | 0 - DMA/C Input Mode 1 | 1 - DMT Input Mode, Input Data = 0

TABLE 6.2 (continued)

PRMXX	DESCRIPTION OF ACTION
07	Set "Character Time Interrupt" (FCHTI) if "Character Time Interrupts Enabled"
09 10	These two bits are used to select the source for BI09-16. (Part of "Input Multiplexer") 9 | 10 0 | 0 - Data Set Status i.e., DSSOB-15 (model 5054) or DSS12-15 (model 5002, 5004) 0 | 1 - RD9-16. This will be the "Transmit Character" fetch from CPU 1 | 0 - UART status register. This is for a "UART Status" DMA/DMC input to CPU 1 | 1 - "Received Data Register" FRD01-08. This is for a "Received Data" DMA/DMC input to CPU
11 12	These two bits select which of three clocks will load RPM01-24 11 | 12 0 | 0 - CLOCKC+. This is a clock generated within the AMLC. 0 | 1 - DENAE. This is a signal from the DMX logic. The leading edge of this signal will remove the DMX request CNDRQ except where to consecutive DMA/C requests are being made. 1 | 0 - 1 | 1 - MYDST+. This is the strobe generated by the CPU during a DMX cycle.
13	1 = Enables the loading of RD01-16 with MYDST+.
14	Reset FMICRE and clear "Received Data" and "UART Status" register
15	1 ⇒ PRMA0-4 = RPM16-20 0 ⇒ PRMA0-4 = (RPM16-20) + 1 If No Skip OR = (RPM16-20) + 2 If Skip

PRMXX	DESCRIPTION OF ACTION
16 17 18 19 20	PROM address field, see PRM15
21	1 ⇒ PRMA0-4 = (RPM16-20) + 2 If condition selected by PRM 22, 23 & 24 is true (i.e., SKIP)
22 23 24	Address of 1 of 8 "Skip if" Conditions 22 | 23 | 24 0 | 0 | 0 Transmit Enabled 0 | 0 | 1 GTXBE Not True 0 | 1 | 0 GRCDMX Not True 0 | 1 | 1 GSTDMX Not True 1 | 0 | 0 DAT01, 02 or 03 Not True 1 | 0 | 1 GECHM Not True 1 | 1 | 0 FIOBY Not Set 1 | 1 | 1 Receive Data Not AVailable (FRDAV Not Set)

AMLC P-ROM. TABLE 6.3.5.

ADDRESS OCTAL	PRMA 4	3	2	1	0	DIP LOCATION / OUTPUTS — PRM BIT - SUB-ROUTINE	10F (W.W) / 7F (E.V). B7	B6	B5	B4	B3	B2	B1	B0	12F (W.W) / 13F (E.V) B7	B6	B5	B4	B3	B2	B1	B0	14F (W.W) / 7G (E.V). B7	B6	B5	B4	B3	B2	B1	B0	COMMENTS.
							24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	
00	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
01	0	0	0	0	1		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NO-OP.
02	0	0	0	1	0		0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SKIP IF [FIOBY NOT SET]
03	0	0	0	1	1		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	FIOBY SET. OUTPUT STROBE (CONFIG, LINE CONTROL OR DSC)
04	0	0	1	0	0		0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SKIP IF [NO RECEIVE DATA FOR INPUT TO CPU]
05	0	0	1	0	1		0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	JUMP TO RCR. & RESET DATA AVAILABLE.
06	0	0	1	1	0		1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SKIP IF [NO RECEIVE STATUS FOR INPUT TO CPU]
07	0	0	1	1	1		0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	JUMP TO STR. & RESET DATA AVAILABLE.
10	0	1	0	0	0		1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SKIP IF [RECEIVE DATA NOT AVAILABLE]
11	0	1	0	0	1		0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	RESET DATA AVAILABLE.
12	0	1	0	1	0	SKTX	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SKIP IF [TRANSMIT BUFFER NOT EMPTY]
13	0	1	0	1	1		0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	JUMP TO TXR.
14	0	1	1	0	0		0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	JUMP TO ZERO & RESET FMICRE & REGISTERS.
15	0	1	1	0	1	RCR	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SKIP IF [NOT ECHO]
16	0	1	1	1	0		0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	ECHO. OUTPUT RDATA TO UART WITH DATA LOAD STROBE.
17	0	1	1	1	1		1	1	0	1	1	1	1	1	0	0	0	0	1	0	1	1	0	0	0	1	1	0	0	0	SKIP IF [NO RECEIVE STATUS], SET DMX REQUEST, SELECT DENAE CLOCK (LE).
20	1	0	0	0	0		0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	JUMP TO STRA, SELECT MYDST CLOCK, REMOVE DMX REQUEST.
21	1	0	0	0	1		0	0	0	0	0	1	0	1	0	1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	JUMP TO SKTX, SELECT MYDST CLOCK.
22	1	0	0	1	0	STR	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SKIP IF [NOT ECHO]
23	1	0	0	1	1		0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	ECHO. OUTPUT BREAK CHAR TO UART.
24	1	0	1	0	0	STRA	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	0	0	1	1	0	0	0	SET : DMX REQUEST. SELECT DENAE CLOCK (LE).
25	1	0	1	0	1		0	0	0	0	0	1	0	1	0	1	0	0	1	1	0	1	0	0	0	1	0	0	0	0	JUMP TO SKTX, REMOVE DMX REQUEST. SELECT MYDST CLOCK.
26	1	0	1	1	0	TXR	0	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SKIP IF [TRANSMIT ENABLED].
27	1	0	1	1	1		0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	TX NOT ENB. OUTPUT MARK CHAR TO UART. CLEAR & JMP → ZERO.
30	1	1	0	0	0		0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0.	0	1	0	1	0	0	0	TX ENB. SET DMT REQUEST, SELECT DENAE CLOCK.
31	1	1	0	0	1		0	0	1	1	1	0	0	1	1	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	SKIP IF [DAT01, 02 OR 03 $\overline{\text{EQUAL}}$ 1], SELECT MYDST CLOCK.
32	1	1	0	1	0		0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	0	0	0	1	1	1	0	0	0	JUMP +2, SET DMT REQUEST, FORCE INPUT DATA TO ZERO, SELECT DENAE CLK.
33	1	1	0	1	1		0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	JUMP +2.
34	1	1	1	0	0		0	0	0	0	0	0	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	SELECT MYDST CLOCK.
35	1	1	1	0	1		0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	1	1	1	OUTPUT RD REGISTER → UART, CLEAR & JUMP TO ZERO.
36	1	1	1	1	0																										} SPARE.
37	1	1	1	1	1																										

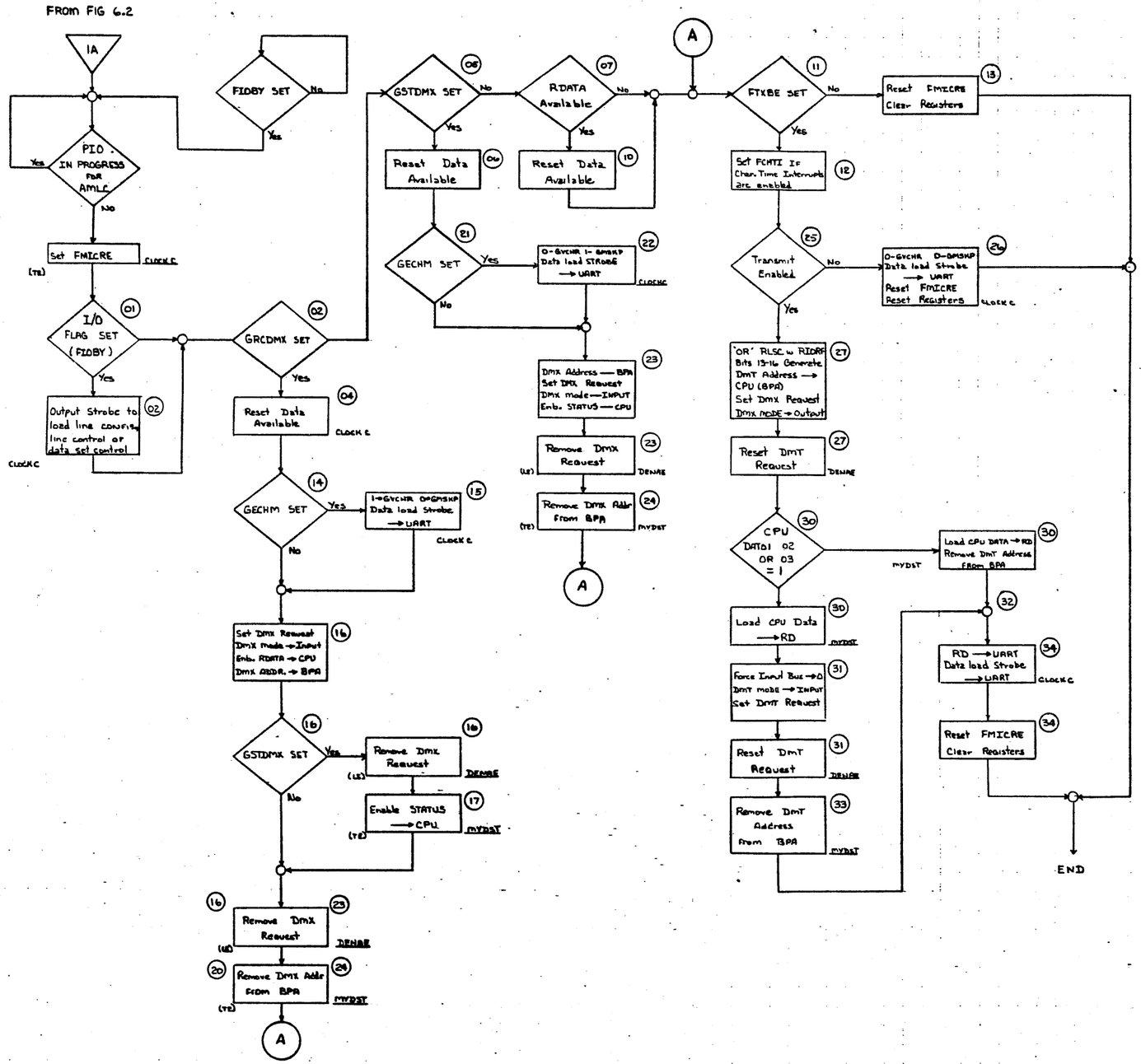


FIGURE 6.5
AMLC MAIN CONTROL
FLOW CHART

bit 15 of the DMA/C address (9/R10). FDMCHX being set will invert ADD15.

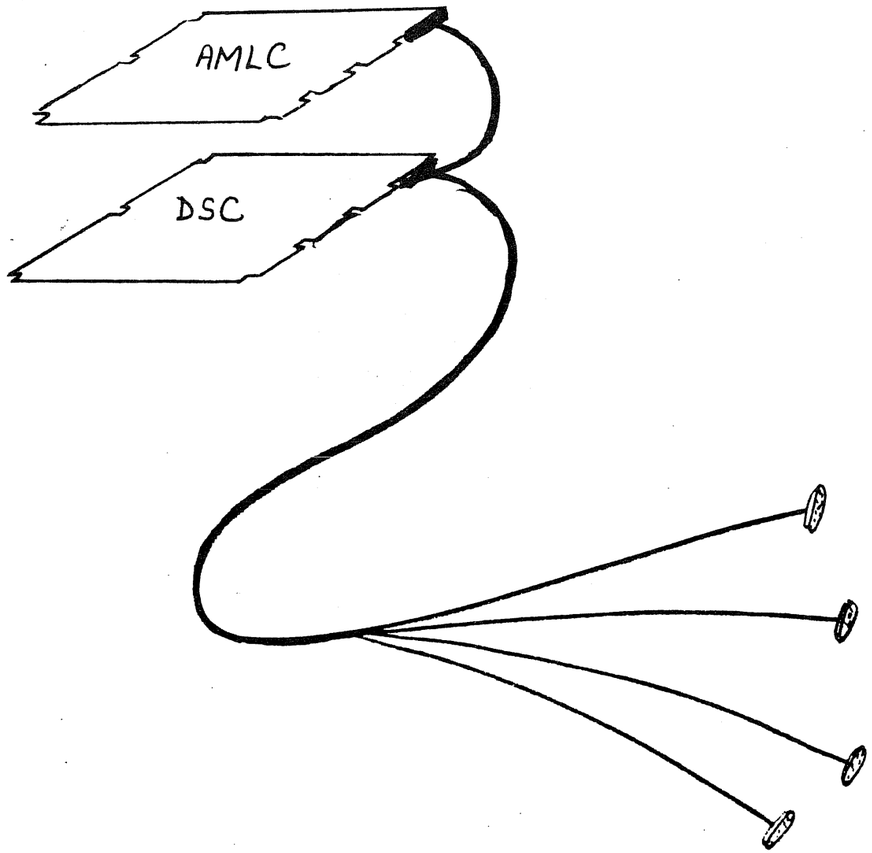
When an "End of Range" occurs the DEORF is set, and when the DENAP- goes low FEORF (8/D13) is set. FEORF setting will toggle FDMXCH causing the Receive Buffer channel address to be changed.

An INA'0754 will reset DEORF and FEORF and it is necessary that the software clear out the Receive Buffer not in use before the next "End of Range".

6.6 AMLC with Data Set Control

The AMLC models 5002 or 5004 are the Data Set Control versions of the AMLC. They consist of one AMLC and one DSC board and are cabled together as shown in figure 6.6.

FIGURE 6.6



Additional logic is required on the AMLC board (LBD 27). This logic will select the correct line on the DSC board to output the four bits of Data Set Control or to input Data Set Status (4 bits).

The DSC board consists of four groups of logic. Each group will service four lines and consists of four registers with EIA output for the four DSC bits and a four to one input multiplexes for the four DSS bits.

The four DSC bits and the four DSS bits are output/input over a bidirectional bus DSCSA, DSCSB, DSCSC, DSCSD.

The logic on the AMLC (LBD 27) is very simple. At 27/D02 is the RAM used to store Data Set Status (DSS) when a change of status (DSS) occurs. At 27/B07 is the comparator used to compare previously stored status with preset status. At 27/G10 is FSCINT which is set for a change of DSS interrupt.

At 27/M02 are ADRAA- and ADRAB- which go to all four groups on the DSC to provide an address to select one of four lines in each group.

The logic at 27/W05 further decodes the line number to select one of four DSC groups. Also generated are four load pulses used to output DSC to a line.

The Tri-State driver at 27/S08 is used to output DSC over the bidirectional bus between the AMLC and DSC boards.

The register at 27/W13 is used to store three line numbers for a "change of status" interrupt. The register at 27/F13 is used to store DSS and two bits of the line number in response to an OTA'0054.

6.6.1 Output Data Set Control (DSC)

An OTA'0354 will load four DSC bits into RD12-16, the line number into RD1-4 and set FIOBY.

The common control logic will generate an EWDSC- strobe pulse and this will cause one of four LOAD pulses dependent up line number (i.e., RD1-4 control GLSC0-3). GLSC2 and 3 are also decoded to produce one of four SELECT signals. RD13-16 are gated via the Tri-State driver to the DSC board and the SLOAD pulse loads 1 of 16 registers on the DSC board.

6.6.2 Output Line Number to Read DSS

An OTA'0054 will load a line number into RD1-4 and set FIOBY.

The Common Control Logic will generate an ERDSS- pulse which will load current Data Set Status (DSS) into the register at 27/F13. The DSS may now be read by an INA'0054.

6.6.3 Change of Data Set Status

Every time the Line Scan addresses a line the current status (DSS) DSSA-D is compared with previous status ODSSA-D.

If the status has changed SSCHG+ (27/D07) will go high and set FSCINT causing a CPU interrupt. The line number is set into a register SCINO-3 (27/W13), the new status is written into the RAM (27/D03) and FSCINT+B is set. With FSINT+B set the status compare logic is frozen until the CPU, acknowledging the interrupt, executes an INA'0754 which will reset FSCINT. FSCINT+B will reset to the reset CLOCKD+ and free up the status compare logic.

6.6.4 Jumper DIPs on DSC Board

There are four jumper DIPs provided on the DSC Board to enable the user to provide control of the "Local Mode" lead on a type 103F data set.

Figure 6.7.a shows the jumper arrangement for one line.

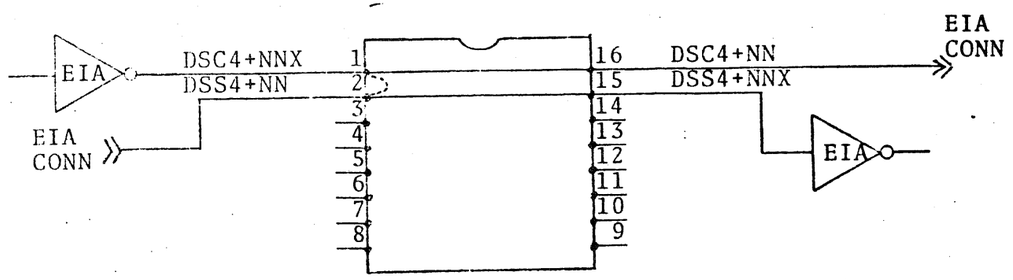
Figure 6.7.b is a table showing DIP Site/Header Run/Line # assignment.

6.7 20 ma Current Loop Interface

By replacing various DIPs with resistors it is possible to convert the AMLC output to 20 ma Current Loop instead of EIA RS232- .

The logic/circuit for each line interface is shown in figure 6.8.

FIGURE 6.7.a

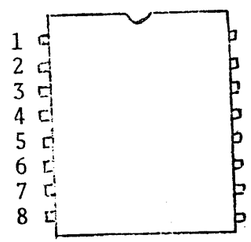


normal jumpers

jumper to enable control of "Local Mode"

FIGURE 6.7.b

JUMPER/LINE ASSIGNMENT



	DIPSITE/LINE # JUMPER ASSIGNMENT			
	43L	29M	14L	6L
16 15	0	4	8	12
14 13	1	5	9	13
12 11	2	6	10	14
10 9	3	7	11	15

FIGURE 6.7. AMLC DATA SET CONTROL.

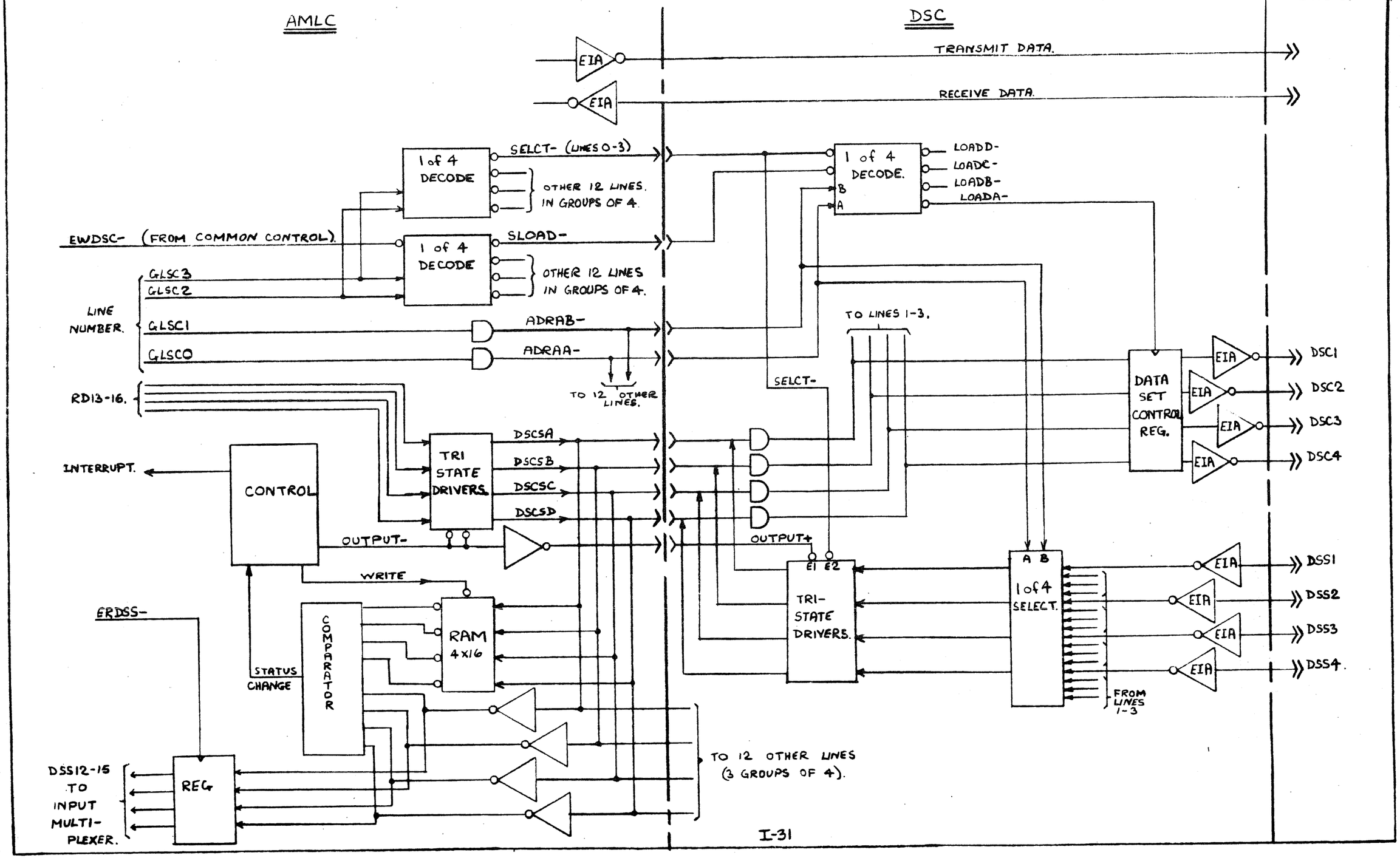


FIGURE 6.8(a). TRANSMIT LOGIC. (See Table 6.4)

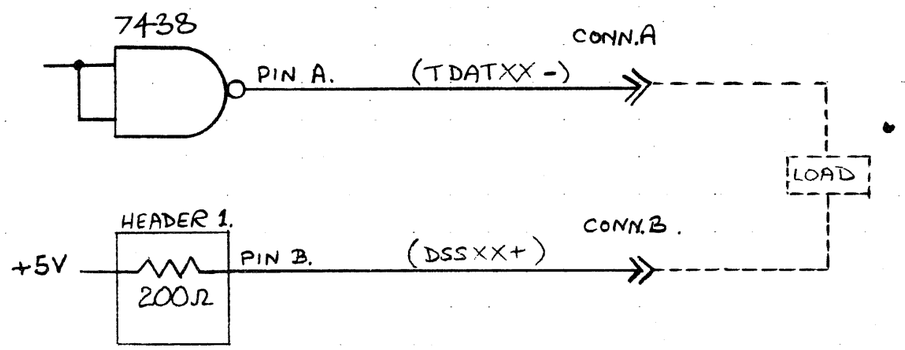
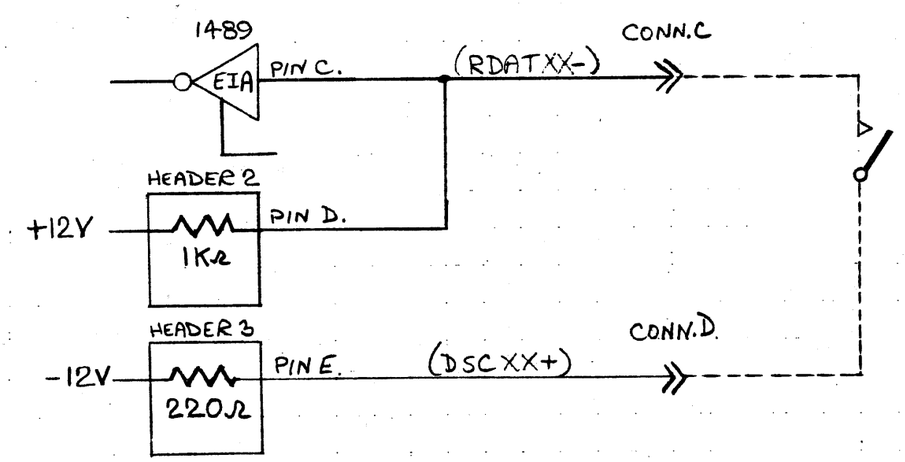


FIGURE 6.8(b). RECEIVE LOGIC. (See Table 6.4)



The 7438 DIP is plugged in a direct replacement for the 1488 DIPs used to interface Transmit Data. Changing jumpers on the Header Dip at SIP will remove ±12 v supply and substitute +5 v.

The 200 ~ resistors are on a Header (Header 1) which is substituted for the 1489 DIP used to interface Data Set Status.

The Receive EIA interface DIP remains unchanged.

The 1K resistors are provided on two Resistor DIPs (one per 8 lines)(Header 2).

The 220 resistors are on a Header DIP (Header 3) which is substituted for the 1488 DIPs used to interface Data Set Control.

The Pin and DIP site assignments are shown in Table 6.4. It should be noted that while model 5075 has only eight lines of Current Loop, the AMLC has provisions for 16 if the need arises.

TABLE 6.4.a (Refer to Figure 6.8)

Line #	7438 Site/ Pin A	Header 1 Site/ Pin B	1489 Site/ Pin C	Header 2 Site/ Pin D	Header 3 Site/ Pin E	Conn A,B,C,D
00	45P/03 49N/03	41P/01 39G/12	43P/01 47H/10	33P/01 41H/13	37N/03 47N/03	CC-15 CC-29 CC-33 CC-09
01	45P/08 49N/08	41P/10 39G/01	43P/10 47H/01	33P/02 41H/15	37N/08 47N/10	CC-17 CC-27 CC-35 CC-07
02	45P/06 49N/06	41P/04 39G/15	43P/04 47H/04	33P/03 41H/12	37N/06 47N/06	CC-11 CC-25 CC-39 CC-05
03	45P/11 49N/11	41P/13 39G/04	43P/13 47H/13	33P/04 41H/14	37N/11 47N/13	CC-13 CC-23 CC-41 CC-01
04	35P/03 43H/03	29P/01 23G/04	31P/01 41G/13	33P/05 41H/10	27P/03 43N/03	CD-15 CD-29 CD-33 CD-09
05	35P/08 43H/08	29P/10 23G/01	31P/10 41G/04	33P/06 41H/08	27P/08 43N/10	CD-17 CD-27 CD-35 CD-07
06	35P/06 43H/06	29P/04 23G/15	31P/04 41G/01	33P/07 41H/07	27P/06 43N/06	CD-11 CD-25 CD-39 CD-05
07	35P/11 43H/11	29P/13 23G/12	31P/13 41G/10	33P/08 41H/09	27P/11 43N/13	CD-13 CD-23 CD-41 CD-01

Note: 1st Line of Site/Pin identities is for wire wrap version
2nd Line of Site/Pin identities is for etch version
Both versions can only change EIA ⟺ 20mA in 8 line groups

TABLE 6.4.b (Refer to Figure 6.8)

Line #	7438 Site/ Pin A	Header 1 Site/ Pin B	1489 Site/ Pin C	Header 2 Site/ Pin D	Header 3 Site/ Pin E	Conn A,B,C,D
08	20P/03 23N/03	16P/01 11K/04	18P/01 9N/10	12P/01 05N/09	16N/03 27N/03	CE-15 CE-29 CE-33 CE-09
09	20P/08 23N/08	16P/10 11K/15	18P/10 3N/13	12P/02 05N/02	16N/08 27N/10	CE-17 CE-27 CE-35 CE-07
10	20P/06 23N/06	16P/04 11K/01	18P/04 9N/01	12P/03 05N/15	16N/06 27N/06	CE-11 CE-25 CE-39 CE-05
11	20P/11 23N/11	16P/13 11K/12	18P/13 9N/13	12P/04 05N/14	16N/11 27N/13	CE-13 CE-23 CE-41 CE-01
12	10P/03 7N/03	06P/01 5H/15	08P/01 3N/04	12P/05 05N/01	02L/03 13N/03	CF-15 CF-29 CF-33 CF-09
13	10P/08 7N/08	06P/10 5H/04	08P/10 3N/01	12P/06 05N/12	02L/08 13N/10	CF-17 CF-27 CF-35 CF-07
14	10P/06 7N/06	06P/04 5H/01	08P/04 3N/10	12P/07 05N/05	02L/06 13N/06	CF-11 CF-25 CF-39 CF-05
15	10P/11 7N/11	06P/13 5H/12	08P/13 9N/04	12P/08 05N/13	02L/11 13N/13	CF-13 CF-23 CF-41 CF-01

7. SIGNAL MNEMONIC

There are two lists, one for the AMLC board and one for the DSC board. The + and - notation has been missed off.

The LBD and cross reference of the signal source is shown as below:

N/AM

N = LBD number. i.e., 8, 9, etc.

AM = cross reference. i.e., M05, B10, etc.

The AMLC list does not include signals from standard PIO logic.

7.1 SIGNAL MNEMONIC AMLC

Signal Name	Source LBD	Description
OCPST	8/L01	AND of Device Address, OCP and STROBE from CPU.
ODSSA ODSSB ODSSC ODSSD	27/E03	Record of "Data Set Status" stored in a RAM for comparison with current "Data Set Status" On Models 5002, 5004 only.
OT14ST	8/E15	AND of CPU STROBE, OTA, Device Address and Function Code 14.
OTAFN	8/H06	OR of the valid function codes for all OTA instructions recognized by the AMLC. Part of Device 'Ready' logic.
OTAST	8/N04	AND of Device Address, OTA and CPU STROBE.
IN07X	11/C12	NAND of Device Address, INA and Function Code 07.
INAFN	8/H08	OR of the valid function codes for all INA instructions recognized by the AMLC. Part of Device 'Ready' Logic.
ADD01-16	9/F02-11	Contents of RAMA bits 1-16. Can be DMC address (or DMA), DMT address or Interrupt Vector Address depending on RAMA address.
ADRAA ADRAB	27/M02	Address bits used to select 1 of 4 lines. Used to address Data Set Control/Status Logic on DSC board.
ADRSTA ADRSTB	14/E13	CPU Address Bits 9 & 10 stored in AMLC after an OTA instruction. These two bits provide an address to steer a strobe pulse (Configuration, Control, DSC or Read DSS).
BOVRN	19-26	Tri State bus signal. This is the "overrun flag" from 16 UART's. This signal is only true for any UART when that UART is selected, i.e., ERDXX is low.
BI01-08	10/D5 10/D9	OR of line number (for receive data input to CPU) and bits 0-7 of DSS. Part of "data input multiplexer".
BI09-16	10/H3-13 10/M3-13	OR of bits 8-15 of DSS, RD register, UART status register and Receive Data Register. Part of "data input multiplexer", also used to steer data to UART's.

Signal Name	Source LBD	Description
BRD01-08	19-26	Tri State Bus signal. This bus connects "Received Data" from 16 UART's together. These signals are only true for any UART when the specific ERDXX signal is true.
BRDAV	19-26	Tri State Bus signal. This is the "Received Data Available" signal from 16 UART's. This signal is only true for any UART when the specific ERDXX signal is true.
BRDFE	19-26	Tri State Bus signal. This is the "Received Data Framing Error" signal from 16 UART's.
BRDPE	19-26	Tri State Bus signal. This is the "Received Data Parity Error" signal from 16 UART's.
BTXBE	19-26	Tri State Bus signal. This is the "Transmit Buffer Empty" signal from 16 UART's.
CARRY	16-N12	Carry output of ALU used in common control logic.
CHDMC	9/S09	Signal used to complement ADD15 is select 2nd DMA (or DMC) channels for received data.
CL00075	11/V02	16 X 75 baud clock
CL00110	11/V08	16 X 110 baud clock
CL00150	11/P02	16 X 150 baud clock
CL00300	11/P02	16 X 300 baud clock
CL00600	11/P02	16 X 600 baud clock
CL01200	11/P02	16 X 1200 baud clock
CL01345	11/P11	16 X 134.5 baud clock
CL01800	11/P05	16 X 1800 baud clock
CL02400	11/K02	16 X 2400 baud clock
CL04800	11/K02	16 X 4800 baud clock
CL09600	11/K02	16 X 9600 baud clock
CL19200	11/K02	16 X 19200 baud clock

Signal Name	Source LBD	Description
CLOCKA CLOCKB CLOCKC CLOCKD	11/K15	Clocks and timing pulses for common control logic.
CLAS00-07	12/W5-W10	Baud Rate clocks (see above) CLAS04 is the output of the programmable clock.
CLEAR	16/T09	OR of CPU Master Clear, Initialize Flip Flop and Clear output of common control PROM. Used a clear common control logic prior to advancing line scan counter.
CLFINT	27/H08	Signal to set flip flop to signal change of Data Set Status. (model 5002/4 only)
CLK00	11/F02	Output of 1st stage of count-down chain in baud rate clock logic.
CLKAS CLKBS CLKCS CLKDS	11/K05	Clock outputs in baud rate clock logic.
CLKR00-15	19-26	Receive baud rate clocks, 1 per line. Output of 1 of 8 selector.
CLKT00-15	19-26	Transmit baud rate clocks, 1 per line. Output of 1 of 8 selector.
CLKXX	11/F05	Main logic clock OR of crystal clock and TSSTP (OCP Single Step).
CLPRM	15/J12	Clock used to load PROM contents into PROM register (RPM1-24). This is an OR of DENAE, MYDST (both from DMX logic) and of CLOCKC. Selection of source for this clock is controlled by PROM.
CLSCAN	11/V11	Clock used to advance "line scan" counter when CLOCKD+ and SCINH- are both high.
CLSTC	15/C08	Pulse used to load registers to staticize UART status and received data.

Signal Name	Source LBD	Description
CLWRM	11/V14	Clock pulse used to generate write pulse for RAMC during AMLC initialize cycle.
CRY01-13	11, 12	Carry outputs of various counters used to generate baud rate clocks.
DADOK	8/H03	AND of decoded Device Address and PIO signal from CPU.
DADAA DADAB	8/F03	Two partialy decoded components of the Device Address.
DATXX		Data bus from PIO logic.
DFCPD	8/F07	Decode of function codes 14, 15, 16 and 17. Part of Ready logic.
DFCPE	14/B10	Decode of function codes 00, 01, 02 and 03. Used to set I/O flag for common control logic and as part of Ready logic.
DPI01-16	10/H,S	Output of "Data Input Multiplexer".
DREDY	8/N08	AMLC "Ready" signal to PIO logic.
DCOO-15	18	Data Set Control bits. One bit per line (Model 5052, 5054 only). EIA interface is shown in LBD No. 18.
DSCSA DSCSB DSCSC DSCSD	27/S09	Bi-directional bus for "Data Set Control" (DSC) and "Data Set Status" (DSS) between AMLC & DSC boards (Models 5001, 5004 only).
DSS00-15	17	Data Set Status bits (one per line).
E50024	8/S06	Signal generated when additional DSC logic is provided on AMLC. Used to differentiate between models 5002/4 and 5052/4.
E5054	23/C05	This signal is true when the upper 8 lines are provided on the AMLC., i.e. on a 16 line not an 8 line AMLC.
DSSA DSSB DSSC DSSD	27/W09	Four data set status bits from DSC board. Models 5002, 5004 only.

Signal Name	Source LBD	Description
ERD00-15	13/DOS	16 bit decode of line scan to select one line (or UART) at a time.
ERDSS	14/J12	"Enable Read DSS". This pulse requested data set status into a register to be read by INA0054. (Models 5002, 5004 only).
ESRDA	14/F11	Decoded PROM command to output a strobe pulse to "Write DSC", "Write Configuration", "Write Control" or "Read DSS".
EWCONF	14/J12	"Enable Write Configuration". Strobe pulse used to output configuration word to 1 of 16 UARTs.
EWDSC	14/J12	"Enable Write DSC". Strobe pulse used to output Data Set Control word to 1 of 16 lines via DSC board. (Models 5002, 5004 only).
EWRMA	14/M10	Write pulse for RAMC. OR of EWRMB and EWRMC.
EWRMB	14/J12	Strobe pulse to write new line control information into RAMC.
EWRMC	14/J13	Strobe pulse to clear RAMC during initialize cycle.
FOVRN	15/F02	"UART Overrun Flag" staticized in "UART Status Register" for use by Common Control Logic.
FIOBY	14/E13	PIO flag. Set by OTA's with a function code of 00, 01, 02, 03. Will cause Common Control Logic to output strobe pulse. Used to Output DSC, Configuration, Line Control and to Read DSS.
FINIT	8/N12	Initialize Flip Flop. Set by an OTA1754. Causes all line control bits to be cleared in RAMC. FINIT resets after one line scan.
FCHTI	14/J02	Character Time Interrupt Flip Flop.
FCHTI	14/J02	Character Time Interrupt Slave Flip Flop. Used to signal fact that two interrupts have occurred before an INA0754.
FDSC00-15	19-26	One output of "Configuration Register" (1 per line). This output is the data set control bit and can be set by an OTA0154.

Signal Name	Source LBD	Description
FEORF	8/D13	Flip Flop set everytime the AMLC gets End of Range on Receive DMA/DMC channel. Is reset by an INA0754.
FLOOPOO-15	19-26	An output of "Configuration Register" (1 per line). These outputs cause Transmit Data to be looped back to become Receive Data for on line test purposes.
FMICRE	15/K09	This Flip Flop is set to enable the PROM common control logic to service a line.
FMSPOO-15	19-26	This Flip Flop is a control function set at the same time as the UART Transmit Buffer is loaded to cause line to mark or space if FVCHR is not set.
FRD01-08	15/F04, 07	8 Bit register used for staticizing Received Data from UARTs.
FRDAV	15/F02	An output of Register used to staticize UART status. This is "Receive Data Available".
FRDFE	15/F02	"Received Data Framing Error". An output of Register used to staticize UART status.
FRDPE	15/F02	"Received Data Parity Error". An output of Register used to staticize UART status.
FRNEN	11/F08	"Run Enable Flip Flop". Enables AMLC to run from crystal clock.
FRSYN	11/H15	Flip Flop to resynchronize internal clocks after control logic has used CPU pulses such as DENAE & MYDST.
FTMDOO-15	19-26	A Flip Flop number (1 per line) that controls Transmit Data out to EIA interface.
FVCHOO-15	19-26	Valid character Flip Flop (1 per line). This Flip is set if bit 1 in the CPU word containing transmit character is set. If this Flip Flop is reset data out will be mark or space and not a normal character.
GINIT	8/K11	Decoded OCP1754 with CPU strobe. This is the initialize instruction from the CPU.

Signal Name	Source LBD	Description
FINST-A	14/E04	Decode of INA0754 and Strobe. This signal clears EOR Flip Flop and"Character Time Interrupt" Flip Flops.
GINT	14/N03	AMLC Interrupt. This signal is ANDED with FMASK+ to interrupt CPU.
GINTE	14/M01	Part of AMLC interrupt logic. OR of "Character Time Interrupt" and "Change of Data Set Status Interrupt" (Model 5002, 5004).
GBRK	15/K05	Decode of UART status and Line Control word to indicate AMLC has received a Break Character.
GCHZR	15/K07	Decode of an "All Zero" Character. Receive only.
GCLR	14/E03	Pulse that loads "Line Number" and "Character Time Interrupt" into status register.
GDBSY	8/G10	"AMLC Busy" signal. This signal true will cause the AMLC to respond "Not Ready" to all PIO except OCP's and INA0754 (Input AMLC Status).
GECHM	15/K05	Decode of "Echo Back Enable", "Valid Character Received" to enable hardware echo of received character.
GLSC0-3	15/X05	4-bit line number. These four bits are an OR of the "Line Scan Counter" and "RD1-4". RD1-4 is the line number from an OTA0054, 0154, 0254 or 0354 instruction.
GMKSP+A GMKSP+B	13/P03	OR of RD2 and RPM03. This signal controls the MARK/SPACE Flip Flop in the "Line Interface Logic" when a new character is output to the UART.
GRCDMX	15/K04	Signal to common control logic to indicate a valid character has been received.
GRDA00-15	13/J03	"Reset Data Available". Sixteen decoded signals to reset UART "Data Available" flags.
GRDFE	10/K15	"Received Data Framing Error". Input to CPU of Framing Error Flag.
GRDPE	10/B15	"Received Data Parity Error". Input to CPU of Parity Error Flag.

Signal Name	Source LBD	Description
GSKIP	16/T04	When this signal is true PROM address will increment by two (2).
GSSTP	11/C06	AND of "NOT NORMAL MODE" & "NOT RUN ENABLE". Used as an enable for OCP "Single Step".
GSTDMX	15/K04	Signal to common control logic to signal that UART status should be reported to CPU. i.e., Break character received, overrun, etc.
GUNRN	16/M04	Underrun signal. i.e., In word from transmit dedicated cell in CPU, bits 1, 2 and 3 were not set.
GVCHR+A GVCHR+B	13/P03	OR of RD1 and RPM02. This signal controls to Valid Character Flip Flop in the "Line Interfact Logic" when a new character is output to the UART.
MODE0 MODE1 MODE2 MODE4	15/S12	Source of signals for CPU mode lines used during PIO, DMX and Interrupt cycles.
MSTCL- MSTCL+X	8	"MASTER CLEAR" Signal. OR of SYSCL and OCP1754.
MSTCL+ MSTCL+A	8	"MASTER CLEAR" Signal. OR of SYSCL and FINIT. Used to reset UARTs.
MUXA1 MUXA2	10/D01 10/D02	Address bits to "Data Input Multiplexer".
PRM01-08 PRM09-16 PRM17-24	16/C03 16/C06 16/C10	PROM with 24 bit word. Used to sequence common control logic.
PRMA0-4	16/N13	PROM address bits from ALU and 1/2 address at 16/T13.
PVLVP		Used to hold unused inputs to Logic 1.
RILN0-3	14/J02	Line number stored in "Character Time Interrupt Register".

Signal Name	Source LBD	Description
RCLA05-16	12/E03 12/E08	12 bit output holding register for programmable clock constant.
RCTIE	14/T07	"Character Time Interrupt Enable". Output of RAMC.
RD01-16	9/M02 9/M05 9/M08 9/M11	Data Buffer Register. Register for temporarily holding data from CPU. Used for Transmit Character (after DMT) and when OTA0054, 0154, 0254 and 0354 instructions are performed.
RDAT00-15	17	Received Data for sixteen lines 00-15.
RECHM	14/T07	"Echo Back Enable". Output of RAMC.
RFI0A1-4	15/S09	Address bits for RAMA. This RAM holds DMA/C address, etc.
RLSC0-3	15/S05	Outputs of Line Scan Counter.
RLSCRY	15/S05	Carry output of Line Scan Counter. Used to Reset the Initialize Flip Flop FINIT.
RPM01-06 RPM07-12 RPM13-18 RPM19-24	16/J03 16/J05 16/J08 16/J11	Holding register (24 bit) for output of PROM.
RRCOL	14/T07	"Receive Off but Report Open Line (or Break)". Output of RAMC.
RRCEN	14/T07	"Receive Enable". Output of RAMC.
RSYN	11/D15	Set/Reset control for FRSYN Flip Flop.
RTXEN	14/T10	"Transmit Enable". Output of RAMC.
SCIN0-3	27/W14	Outputs of register holding line number for "Change of Data Set Status" interrupt. (Model 5002, 5004 only).
SCINH	15/P01	"Scan Inhibit". Halts line scan when a UART needs service or FIOBY is set.
SCKA00-15 SCKB00-15 SCKC00-15	19-26	3 bit output of Line Configuration Register. Used as an address to select 1 of 8 baud rate clocks.

Signal Name	Source LBD	Description
SDCC	16/M02	Select signal used to select source for "Valid Character" and "Mask/Space" signals to Line Interface Logic.
SMICE	15/F09	Set enable for FMICRE.
SSCINT	27/S14	Write pulse to write line number into status register for "Change of Data Set Status" and to write new Data Set Status into RAM (ODSSA, B, C and D). (Models 5002, 5004 only).
SSCHG	27/C08	"Data Set Status Changed". Output of Comparator. (Models 5002, 5004 only).
STXBE	15/C02	Set enable for Transmit buffer empty Flip Flop in UART status register.
TCLK	11/C05	Output of crystal oscillator.
TCLS00-15	13/D08	16 strobe pulses used to load configurations into UART and associated "Line Configuration Register".
TDAT00-15		Transmit Data.
TDL00-15	13/J08	"Transmit Data Load Strobe". One per UART used to load Transmit Character into UART.
TLRD	16/N07	"Load RD Register Strobe". OR of MYDST and OTAST.
TREE00-15	19-26	"Transmit Register Empty". UART output.
TSSTP	11/D07	Decoded OCP0154 with Strobe. (Single Step pulse).
UARST	13/E06	Strobe pulse. Part of "Reset Data Available" and "Transmit Data Load" pulses.
WDSS	27/B03	"Write Data Set Status Strobe". Pulse used to write New DSS into RAM.

7.2 SIGNAL MNEMONIC DSC

Signal Name	Source LBD	Description
OUTPT		Signal from AMLC to put inhibit tri-state drivers on DSC, i.e., put bidirectional bus in output mode.
IDSCA IDSCB IDSCC IDSCD	03/R04 05/R04 07/R04 09/R04	Data Set Status signals, inputs to tri-state drivers.
ADRAA ADRAB		1 of 4 select address from AMLC.
BCLEAR-A BCLEAR-B BCLEAR-C BCLEAR-D	02/D11 04/D11 06/D11 08/D11	Clear DSC signal. This is AMLC CLEAR- signal regenerated.
CLEAR		Clear DSC signal from AMLC.
DSC1+ DSC2+ DSC3+ DSC4+	2,4,6,8	Four "Data Set Control" bits (4 per line) outputs of EIA drivers.
DSC1- DSC2- DSC3- DSC4-	2,4,6,8	Four "Data Set Control" bits, outputs of Data Set Control Registers (one per line).
DSCSA+ DSCSB+ DSCSC+ DSCSD+		Bidirectional bus from AMLC when an A, B, C or D is after + sign. When a 1, 2, 3 or 4 is after the + sign these signals are the outputs of buffer logic on DSC board.
DSS1+ DSS2+ DSS3+ DSS4+		Four "Data Set Status" bits from modem. Line number is after + sign.
DSS1- DSS2- DSS3- DSS4-		Four "Data Set Status" bits, outputs of EIA receivers. Line number is after - sign.
LOADA LOADB LOADC LOADD		Signal from AMLC used to load 1 of 16 "Data Set Control Registers".

Signal Name	Source LBD	Description
SELCT+A SELCT+B SELCT+C SELCT+D		Four signals from AMLC. EAch one selects a group of four lines on the DSC.

8. SOFTWARE AIDS

This section contains outlines for start-up and run routines for the AMLC. They are intended purely as aids to someone writing a driver or a test routine. (See section 8.1, 8.2, 8.3).

Section 8.4 contains some simple routines used in the factory to check out transmit and receive operation. They are intended to run continuously to enable use of an oscilloscope when debugging.

8.1 Start Up Procedure

	Operation	Instruction
1.	Identify all AMLCs in system	INA'11XX
2.	Initialize controller and clear all line control flags in RAMC (i.e., Tx Enable, RcEnable, etc.)	OCP'1754
3.	Set up Transmit DMT Channel. i.e., output base address of block of 16 dedicated cells for transmit characters	OTA'1554
4.	Set up 2 Receive DMA/DMC Channels in CPU	See CPV reference manual
5.	Output Receive DMA/C address to AMLC	OTA'1454
5a.	Set up Vector Address in CPU	
6.	Output Interrupt Vector Address to AMLC	OTA'1654
7.	Set Interrupt Mask	OCP'1554
8.	Output Constant for Programmable Baud Rate Clock	OTA'1754

At this point, if the AMLC configuration is known all lines can be configured by an OTA'0154 and later when it is wished to transmit or receive an OTA'0254

OR

If polling terminals which are not all the same speed or data format, the OTA'0154 (configuration) may be

performed just prior to the OTA'0254 (Transmit Enable, Receive Enable, etc.)

Either way OTA'0154 always precedes OTA'0254.

8.2 Continuation Procedures

These can vary from system to system, but the flow chart in Figure 8.1 will give a general picture.

8.3 Shut-Down Procedure

There is no specific shut-down procedure. Some systems may have Receive Enable on all the time and rely on software recognition of a specific character where initiation of communication is from an outside source.

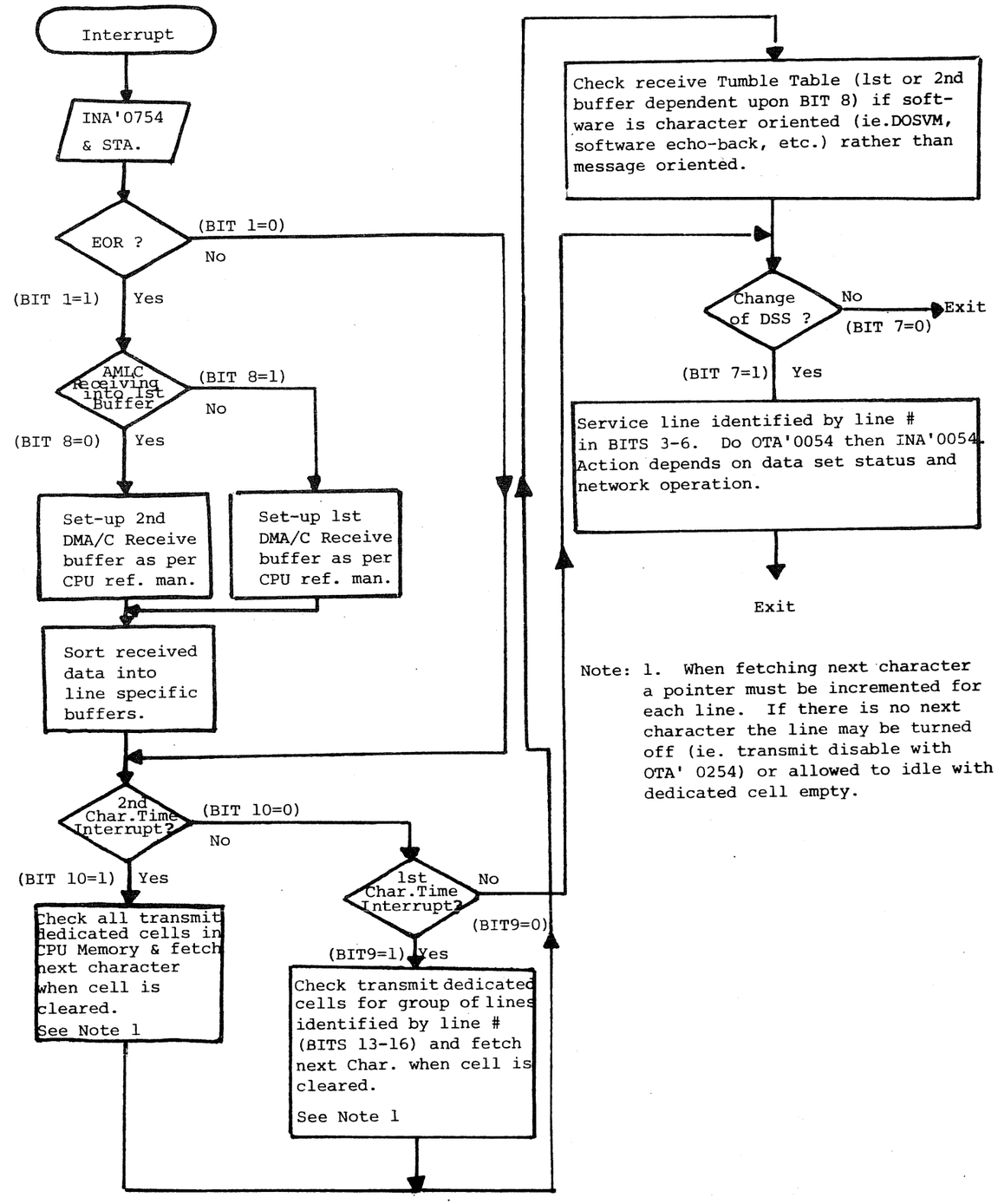
Other systems would always shut down Transmit Enable and Receive Enable when communication with line is not required.

8.4.a Transmit on One Line

```
1000    OCP   1754      Initialize.
   1    LDA   1100
   2    OTA   1554      Output DMT Address.
   3    JMP   1002
   4    LDA   1101
   5    OTA   154       Output Line Configuration.
   6    JMP   1005
   7    LDA   1103      Fetch T Data.
  10    STA*  1100      Store in Dedicated Cell.
  11    LDA   1102
  12    OTA   254       Turn On Transmit.
  13    JMP   1012
  14    LDA*  1100
  15    SZE             Check Dedicated Cell.
  16    JMP   1014      Go Back and Check Again.
  17    LDA   1103      Empty, Fetch Next Character.
  20    STA*  1100      Store in Dedicated Cell.
  21    JMP   1014      Return & Check.
                        Dedicated Cell

1100    20XX            DMT Base Address (AMLC ignores XX).
   1    XX0333          (1200 baud, 2 stops, no parity,
                        8 bit char)
   2    XX0010          (Transmit Enable)  NOTE 1.
   3    100NNN          Transmit Character with valid
                        character bit (bit 1) set.
```


FIGURE 8.1



Note: 1. When fetching next character a pointer must be incremented for each line. If there is no next character the line may be turned off (ie. transmit disable with OTA' 0254) or allowed to idle with dedicated cell empty.

XX = Line Number 00-17 (Octal).

NNN = Transmit Character 000-377 (Octal).

This program will output continuously on the selected line (XX) the character of your choice (NNN).

The data may be observed as TDATXX+. (e.g., TDATOO+ at 19/J05 for line 00) on the oscilloscope. The EIA output (i.e., +12 v to -12 v signal swing) may be checked as TDATXX-.

NOTE 1: If the Line Configuration is changed from XX0333 to XX1333 the transmit character can be observed looped back as RDATXX+A.

8.4.b Transmit and Receive on One Line

```
1000    OCP  1754      Initialize.
   1    LDA  1100
   2    OTA  1554      Output DMT Address.
   3    JMP  1002
   4    LDA  1101
   5    STA  20
   6    STA  21
   7    LDA  1102      Set Up DMA Channels. See Note 1.
  10    STA  21
  11    STA  23
  12    LDA  1103
  13    OTA  1454      Output DMA Channel Address.
  14    JMP  1013
  15    LDA  1104
  16    OTA  154       Output Line Configuration
  17    JMP  1016
  20    LDA  1105
  21    OTA  1654      Output Int. Vect. Address.
  22    JMP  1021
  23    LDA  1106
  24    OTA  254       Turn On Transmit and Receive.
  25    JMP  1024
  26    417
  27    401
  30    OCP  1554      Set Interrupt Mask.
  31    LDA  1107      Fetch T. Character.
  32    STA* 1100      Store in Dedicated Cell.
  33    LDA* 1100      Check Dedicated Cell.
  34    SZE
  35    JMP  1033
  36    INA  1620
  37    STA  1110      Note 2.
  40    LDA* 1110
  41    OTA  1720
  42    JMP  1031      Cell Empty, Fill Again.
```



```
1100    20XX           DMT Address.
   1    177540         (Ten Character Range).
   2    1400           Receive Buffer Base Address.
   3    20             DMA Channel.
   4    XX1333         (1200 baud, 2 stops, no parity,
                       loop, 8 bit character).
   5    1200
   6    XX0011         (Receive and Transmit Enable).
   7    100NNN         Transmit Character.
  10

1200    1300

1300    DAC
   1    SKS  454       Skip If Not Interruption
   2    JMP  1000      Return to 1000.
   3    HLT
```

NOTE 1: Both DMA buffers are set up for the same address.

NOTE 2: The code in locations 1036-1040 enables the contents of any memory location addressed from the sense switches to be displayed on the Control Panel.

XX = Line Number 00 - 17 (Octal).

NNN = Transmit Character 000 - 377 (Octal).

9. CABLING

A variety of cabling arrangements are possible with the AMLC. Figure 9.1 shows an AMLC with the various types of cable used with models 5052, 5054, 5075. The table is an outline description of the various cable types.

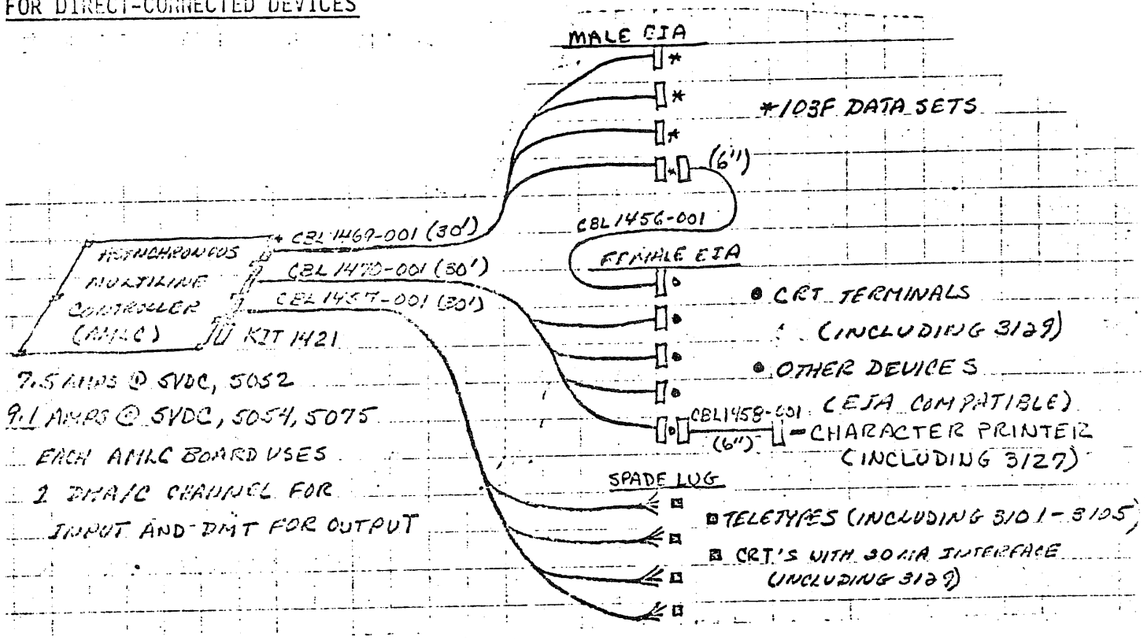
Figure 9.2 shows the cabling arrangements for an AMLC model 5002 (5004 requires four cables). The table is an outline description of the cable and adapters.

Table 9.1 summarizes the various cables and adapters available on the AMLC and shows the pin/connector assignments at the user end.

For more detailed cable information refer to actual cable drawings.

FIGURE 9.1

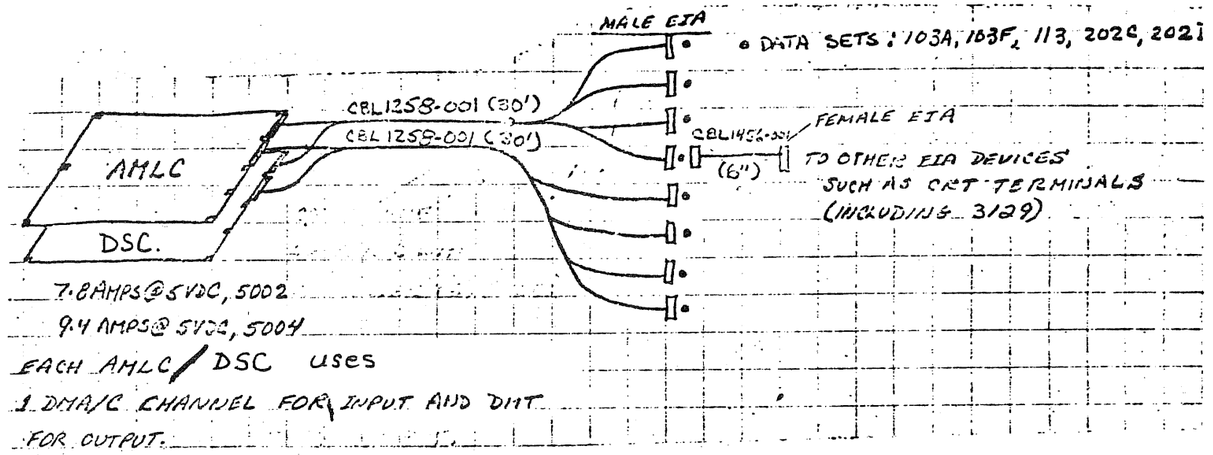
ASYNCHRONOUS MULTILINE CONTROLLERS (AMLC)
FOR DIRECT-CONNECTED DEVICES



Cable Type	Description
CBL1469-001	Cable from AMLC to four male EIA connectors (30').
CBL1470-001	Cable from AMLC to four female EIA connectors (30').
CBL1457-001	Cable from AMLC to four 4-wire spade lug terminations (30'). (for 20 ma current loop)
CBL1456-001	Cable adapter from male EIA to female EIA (6").
CBL1458-001	Cable adapter from female EIA to character printer (6").

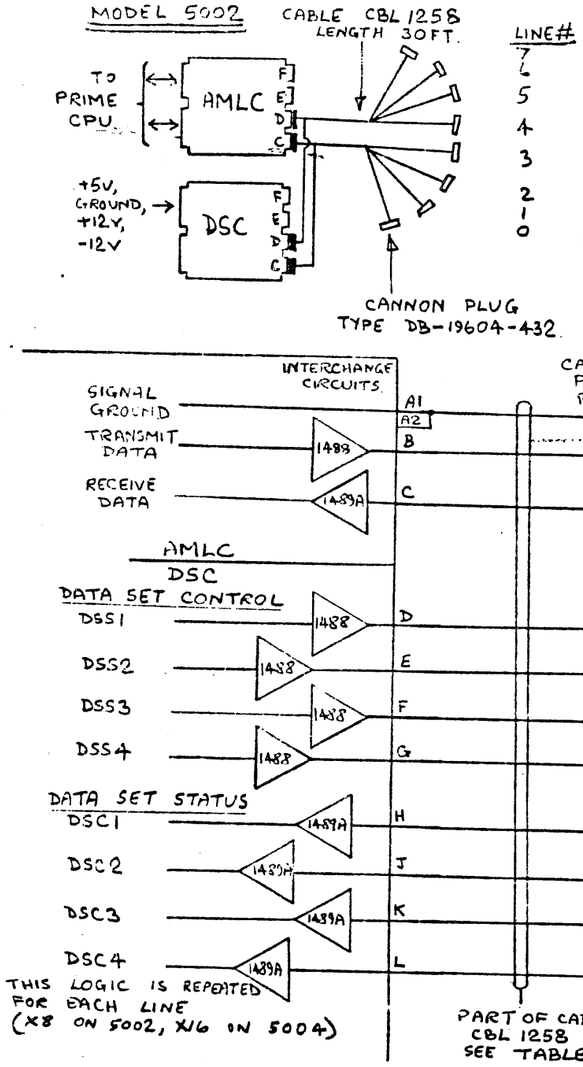
FIGURE 9.2

ASYNCHRONOUS MULTILINE CONTROLLER (AMLC)
FOR TYPE 103/202 DATA SETS



Cable Type	
CBL1258-001	Cable from AMLC and data set controller to four male EIA connectors (30').
CBL1456-001	Cable adapter: male EIA to female EIA (6").

FIG2 MODEL 5002, 5004 AMLC WITH CABLE CBL1258

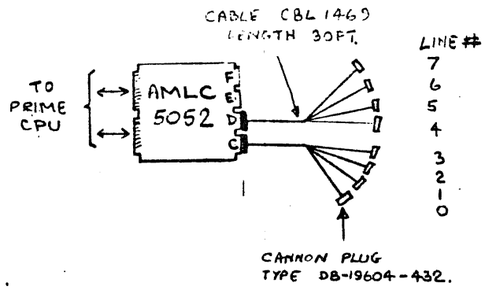


NOTE 1: MODEL 5004 IS IDENTICAL EXCEPT IT REQUIRES FOUR CABLES TO SERVICE 16 LINES.

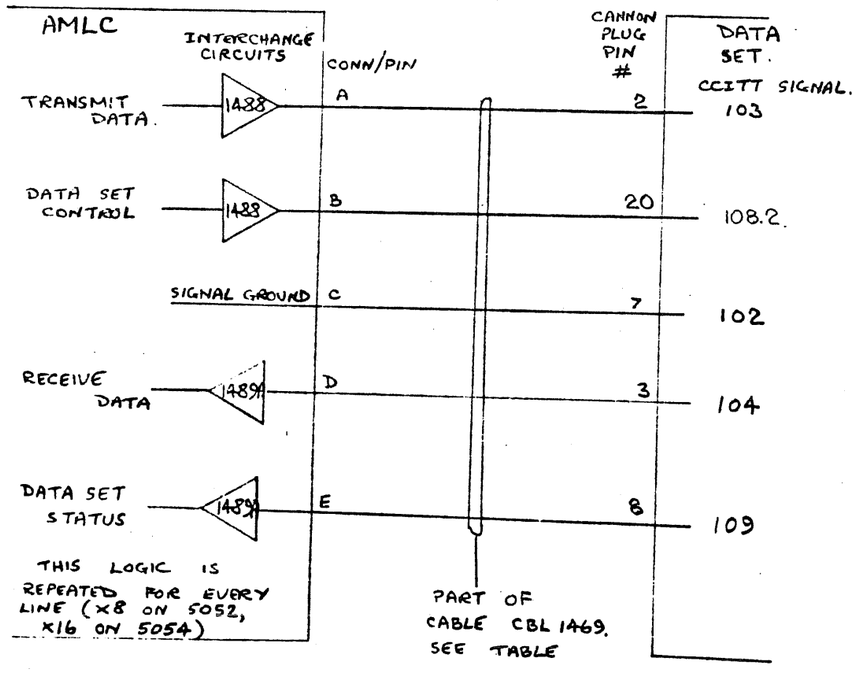
AMLC DSC CONN PIN	LINE # / AMLC CONNECTOR & PIN.																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A (1)	C16	C18	C12	C14	D16	D18	D12	D14	E16	E18	E12	E14	F16	F18	F12	F14	AMLC
A (2)	C34	C36	C40	C42	D34	D36	D40	D42	E34	E36	E40	E42	F34	F36	F40	F42	
B	C15	C17	C11	C13	D15	D17	D11	D13	E15	E17	E11	E13	F15	F17	F11	F13	
C	C33	C35	C39	C41	D33	D35	D39	D41	E33	E35	E39	E41	F33	F35	F39	F41	
D	C13	C21	C29	C37	D13	D21	D29	D37	E13	E21	E29	E37	F13	F21	F29	F37	DSC
E	C14	C22	C30	C38	D14	D22	D30	D38	E14	E22	E30	E38	F14	F22	F30	F38	
F	C15	C23	C31	C39	D15	D23	D31	D39	E15	E23	E31	E39	F15	F23	F31	F39	
G	C16	C24	C32	C40	D16	D24	D32	D40	E16	E24	E32	E40	F16	F24	F32	F40	
H	C17	C25	C33	C41	D17	D25	D33	D41	E17	E25	E33	E41	F17	F25	F33	F41	
J	C18	C26	C34	C42	D18	D26	D31	D42	E18	E26	E34	E42	F18	F26	F34	F42	
K	C19	C27	C35	C43	D19	D27	D35	D43	E19	E27	E35	E43	F19	F27	F35	F43	
L	C20	C28	C36	C44	D20	D28	D36	D44	E20	E28	E36	E44	F20	F28	F36	F44	

NOTE 2. OTHER ASSIGNMENTS OF THE FOUR DSC/DSS LEAD BY MODIFYING THE CABLE.

FIG 1 MODEL 5052, 5054 AMLC WITH CABLE CBL 1469.



NOTE 1: MODEL 5054 IS IDENTICAL EXCEPT IT REQUIRES FOUR CABLES TO SERVICE SIXTEEN LINES.



AMLC CONN PIN	LINE # / AMLC CONNECTOR & PIN #.															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	C15	C17	C11	C13	D15	D17	D11	D13	E15	E17	E11	E13	F15	F17	F11	F13
B	C9	C7	C5	C1	D9	D7	D5	D1	E9	E7	E5	E1	F9	F7	F5	F1
C	C16	C18	C12	C14	D16	D18	D12	D14	E16	E18	E12	E14	F16	F18	F12	E14
D	C33	C35	C39	C41	D33	D35	D39	D41	E33	E35	E39	E41	F33	F35	F39	F41
E	C29	C27	C25	C23	D29	D27	D25	D23	E29	E27	E25	E23	F29	F27	F25	F23

NOTE 2. FOR OTHER ASSIGNMENTS OF DATA SET STATUS (E) AND DATA SET CONTROL (B) MODIFICATIONS MUST BE MADE TO THE CABLE BY REMOVING & REASSIGNING PINS.

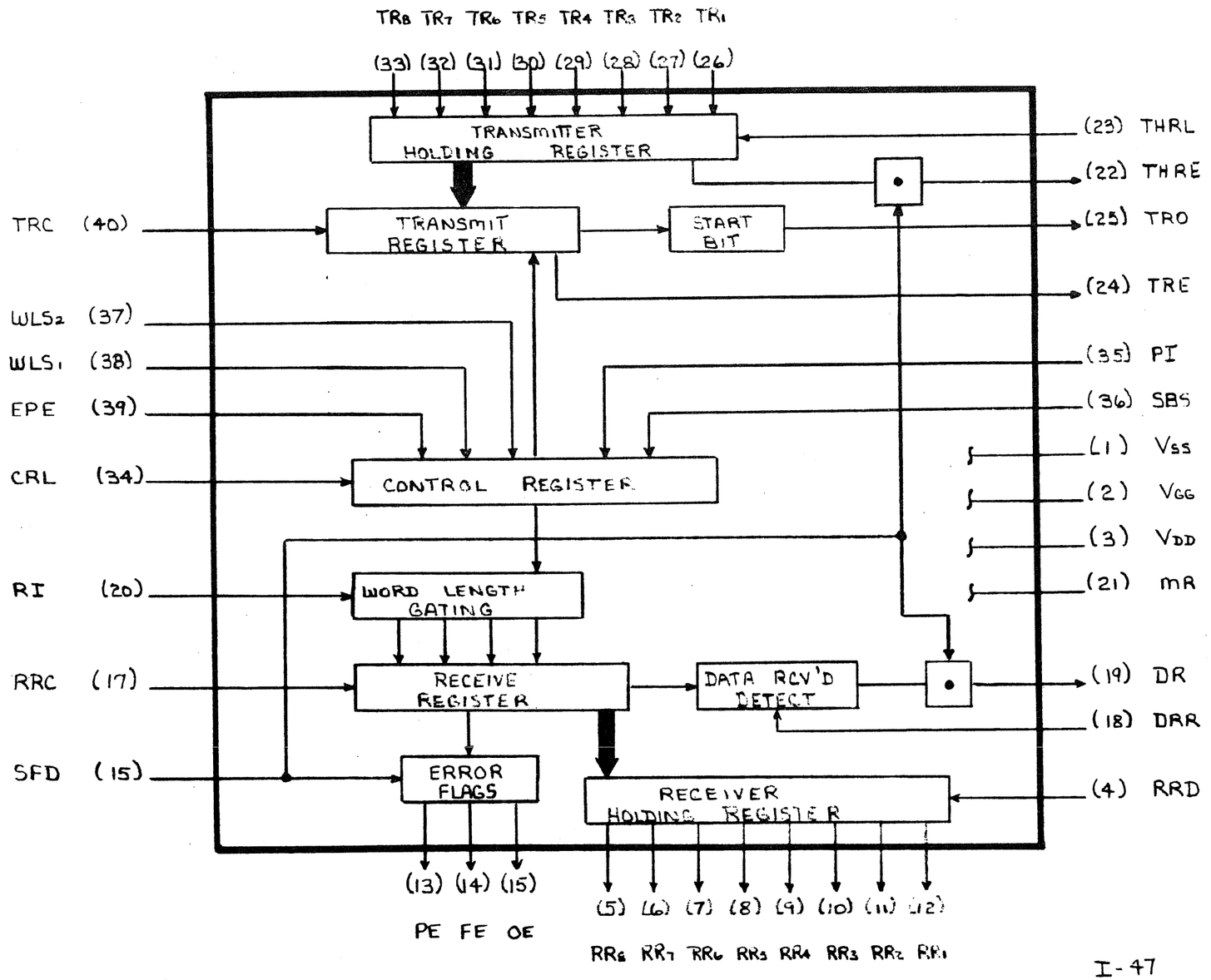
TABLE 9.1

AMLC CABLES, CABLE SIGNAL/CONNECTOR PIN LIST.

CABLE #	SIGNAL / PIN # (AT EIA CONNECTOR)																			
	TRANSMIT	RECEIVE	CONTROL	STATUS	JUMPER.	SIGNAL GROUND	REQ TO SEND	CLEAR TO SEND	DATA SET READY	CARRIER DET	DATA TERM'L READY	SUPERVISORY TRANS DATA	SUPERVISORY REC DATA	TERMINAL BUSY						
CBL1469-001 J1-J4	2	3	4	5	(4→20)	7														
CBL1470-001 J1-J4	3	2	9	20	(20→8) (4→5)	7														
CBL-1456-001 ADAPTS 1469 TO 1470.	3	2	9	20	(20→8) (4→5)	7														
CBL1458-001 ADAPTS 1470 TO CHARACTER PRINTER (3127)	3	2	9	11	(6→8) (8→20)	7														
CBL 1258-001	2	3			(11→14) (12→16)	7	4	5	6	8	20	11	12	25						
CBL 1457-001	✓	✓				✓	}													
	✓	✓																		

✓ = LUG TERMINATION

The table above summarizes cable signal/connector pin assignments for standard cables between AMLC and serial I/O devices and data sets. All connectors, except lug terminations, are EIA-compatible.


TR8 TR7 TR6 TR5 TR4 TR3 TR2 TR1
(33) (32) (31) (30) (29) (28) (27) (26)
TRANSMITTER HOLDING REGISTER
TRANSMIT REGISTER
START BIT
CONTROL REGISTER
WORD LENGTH GATING
RECEIVE REGISTER
DATA RCV'D DETECT
ERROR FLAGS
RECEIVER HOLDING REGISTER
TRC (40)
WLS2 (37)
WLS1 (38)
EPE (39)
CRL (34)
RI (20)
RRC (17)
SFD (15)
(23) THRL
(22) THRE
(25) TRO
(24) TRE
(35) PI
(36) SBS
(1) VSS
(2) VGG
(3) VDD
(21) mR
(19) DR
(18) DRR
(4) RRD
(13) (14) (15)
PE FE OE
(5) (6) (7) (8) (9) (10) (11) (12)
RR6 RR7 RR0 RR3 RR4 RR3 RR2 RR1

PIN#	SYMBOL	NAME	DESCRIPTION
(1)	Vss	+5v Supply	
(2)	Vgg	-12v Supply	
(3)	Vdd	Ground	
(4)	RRD	Receive Register Disconnect	disconnects holding reg.outputs from RR8-RR1 data outputs
(5-12)	RRx	Receive Holding Register Data	character right justified RR1=LSB, parallel
(13)	PE	Parity Error	received data parity
(14)	FE	Framing Error	received character has no valid stop bit
(15)	OE	Overrun Error	previously received character was not read (DR not reset) before the present character was transferred to Rec.Holding Register
(16)	SFD	Status Flags Disconnect	disconnects PE, FE, OE & THRE outputs
(17)	RRC	Receiver Register Clock	16 times faster than desired receiver shift rate
(18)	DRR	Data Received Reset	resets DR line
(19)	DR	Data Received	entire character has been received & transferred to Rec.Holding Reg.
(20)	RI	Receiver Input	serial input data; enters Rec.Reg.as determined by character length, parity & no. of stop bits; high level when data is not being received
(21)	MR	Master Reset	clears logic after power on; resets all registers & sets serial output to a high level output voltage
(22)	THRE	Trans.Holding Reg.Empty	Holding Reg.has transferred its contents to Trans. Reg.& thus may be loaded with a new character.

PIN#	SYMBOL	NAME	DESCRIPTION
(23)	THRL	Trans.Holding Reg.Load	when low enter character into Trans.Holding Reg. low to high transfer character to Trans.Reg. (if Trans.Reg. is not in process of transmitting a character)*
(24)	TRE	Trans.Reg.Empty	Trans.Reg. has completed serial transmission of full character including stop bits (remains at high level until start of transmission of next character)
(25)	TRO	Trans.Reg.Output	Contents of Trans.Reg.serially shifted out on this line
(26-33)	TRx	Trans.Reg.Data Inputs	parallel 8-bit character input to Trans.Holding Reg.
(34)	CRL	Control Reg.Load	loads Control Reg.with control bits
(35)	PI	Parity Inhibit	inhibits parity generation and verification
(36)	SBS	Stop Bit(s) Select	selects # of Stop Bits generated after Parity Bit during transmission; HI=two stop bits LO=single stop bit
(37-38)	WLSx	Word Length Select	Combination of these two bits selects 1 of 4 character length
(39)	EPE	Even Parity Enable	selects even/odd parity HI=even LO=odd
(40)	TRC	Trans.Reg.Clock	16 times faster than desired transmitter shift rate

*If a character is being transmitted the transfer is delayed until its transmission is completed, when completed new character transferred simultaneously with the initiation of the serial transmission of the new character.

LTR	DATE	REVISION	DR.	CK.

SHEETS

OPTION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
5002	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X					X			X	X		X								
5004	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X			X		X									
5052	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X					X			X				X							
5054	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X				X					X						
5074	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X			X	X	X	X	X	X	X	X		X	X	X						X					
5075	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X		X		X							X				
5072	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X			X	X	X	X						X		X								X			

WIRE LIST	

MATERIAL	
UNLESS OTHERWISE SPECIFIED – REMOVE ALL BURRS AND SHARP EDGES: – DIMENSIONS ARE IN INCHES – TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	
DWN N. Bryan 4/17/75	
CHK H.B. McGrath	
ENG 23.4.75.	
APPRD	
USED ON	
NEXT ASSY	

PRIME COMPUTER, INC.
NATICK, MASS.

DIRECTORY
AMLC
EV

SCALE	SIZE	DWG. NO.	REV.
SHEET OF	C	LBD1735	C

II-1

REVISION LEVEL

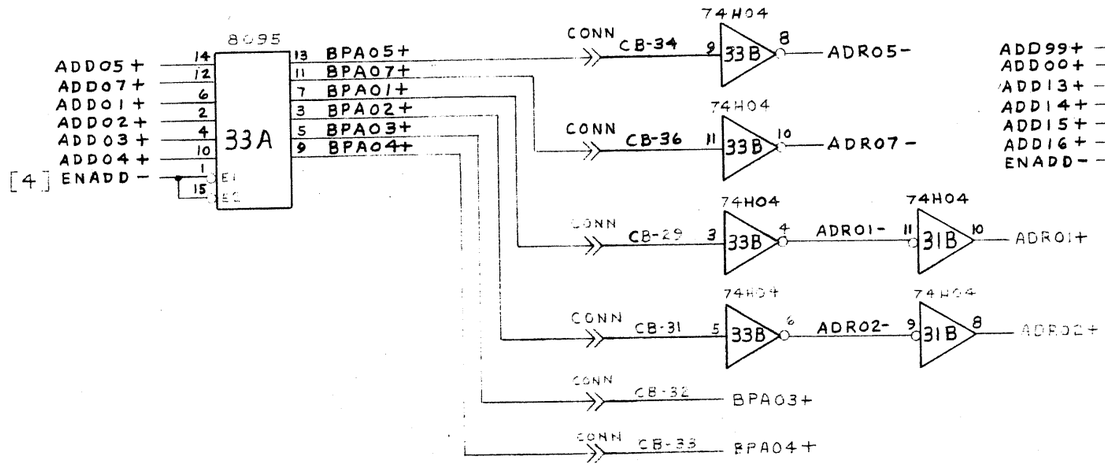
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	DATE	ENGINEERING CHANGE NOTICES
A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A						1/31/75	RELEASED
B								B							B		B	B				B						B	B	B							B	B				4/23/75	PER ECN 1575
C																																	B								6/3/75	PER ECN 1602
D								C																																		7/7/75	PER ECN 1609
E																															B	B									11/20/75	PER ECN 1618
E																																					A				11/14/75	SHEET 37 ADDED
F																															C	C	C	B	C	C					1/30/76	PER ECN 1723-A
G								D			B				B	C		C		B		B	C	B																	3/17/76	PER ECR 1747
H			B																																D	D	B				7/30/76	PER ECR 1857
J								E	B	B	C	B	B	C		B	D	C	C	B	C	D	C	B	B	B	C				D	D	D	C	E	E	C				11/30/76	PER ECR 1908

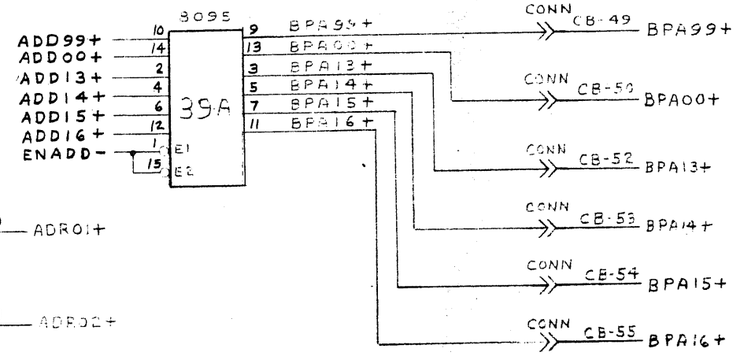
LTR	DATE	REVISION	DR.	CK.

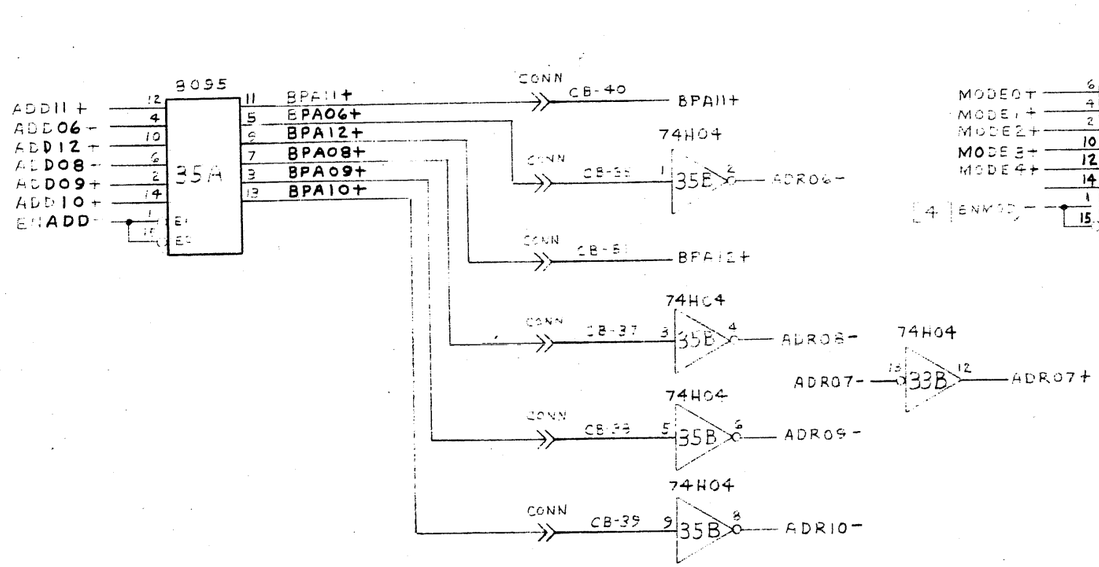
PB	1/31/75			
4/28	4/28			
5/8	5/8			
P.B.	7/7/75			
JPL	11/20/75			
11/14	11/14/75			
J.T.S.	1/30/76			
GJ	3/17/76			
J.T.S.	7/30/76			
JPL	11/30/76			

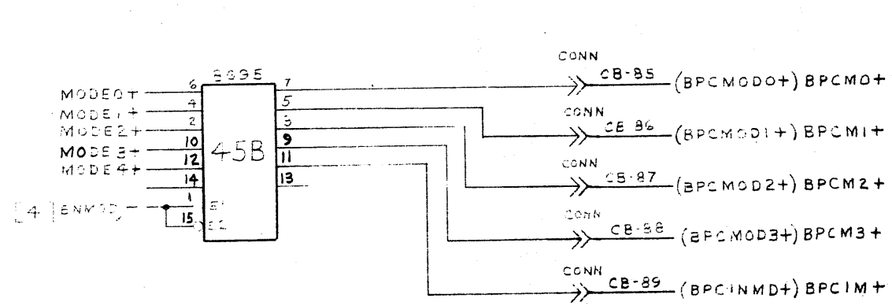
MATERIAL	DWN Paul Beatrice 10-11-74	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ± 1/2°	CHK 1/31/75	REVISION STATUS SHEET AMLC E.V.	
	ENG 1.31.75		
	APPR		
	USED ON NEXT ASSY	SCALE SHEET 1 OF 35	SIZE C DWG. NO. LBD1735 REV. J

II-2







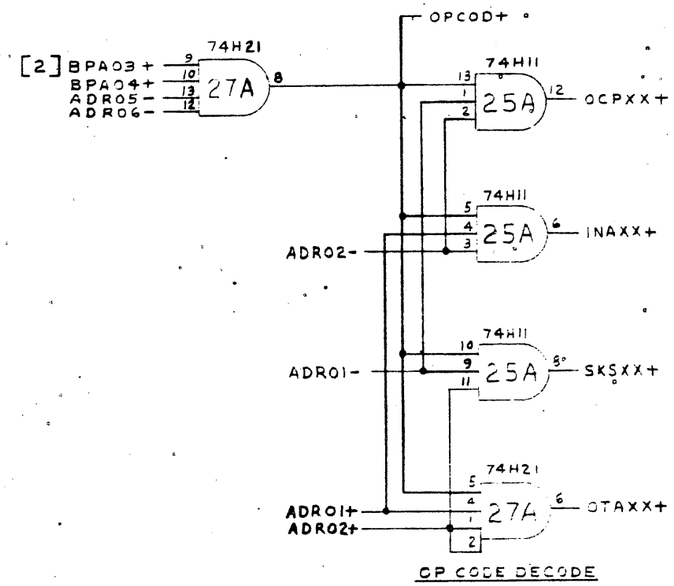


LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
ADD99+	GD29A	—
ADD00+	GD29A	—
MODE0+	MODE0+	015
MODE1+	MODE1+	015
MODE2+	MODE2+	015
MODE3+	GD45B	
MODE4+	MODE4+	015

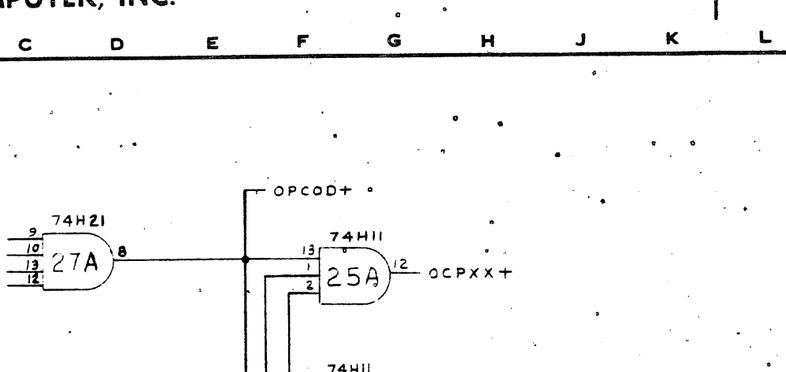
I/O BUS ADDRESS
DRIVERS & RECEIVERS

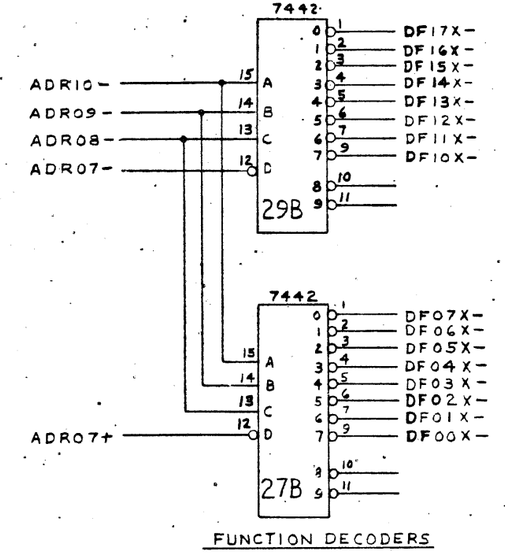
MATERIAL	DWN 3/14/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	CHK	I/O BUS INTERFACE LOGIC ADDRESS AND MODE LINES AMLC
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 2 OF
		SIZE C / DWG. NO. LBD1735 / REV. EV A

PDF-003

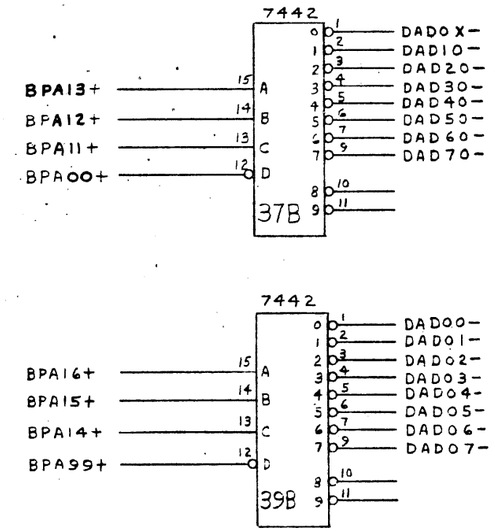


OP CODE DECODE





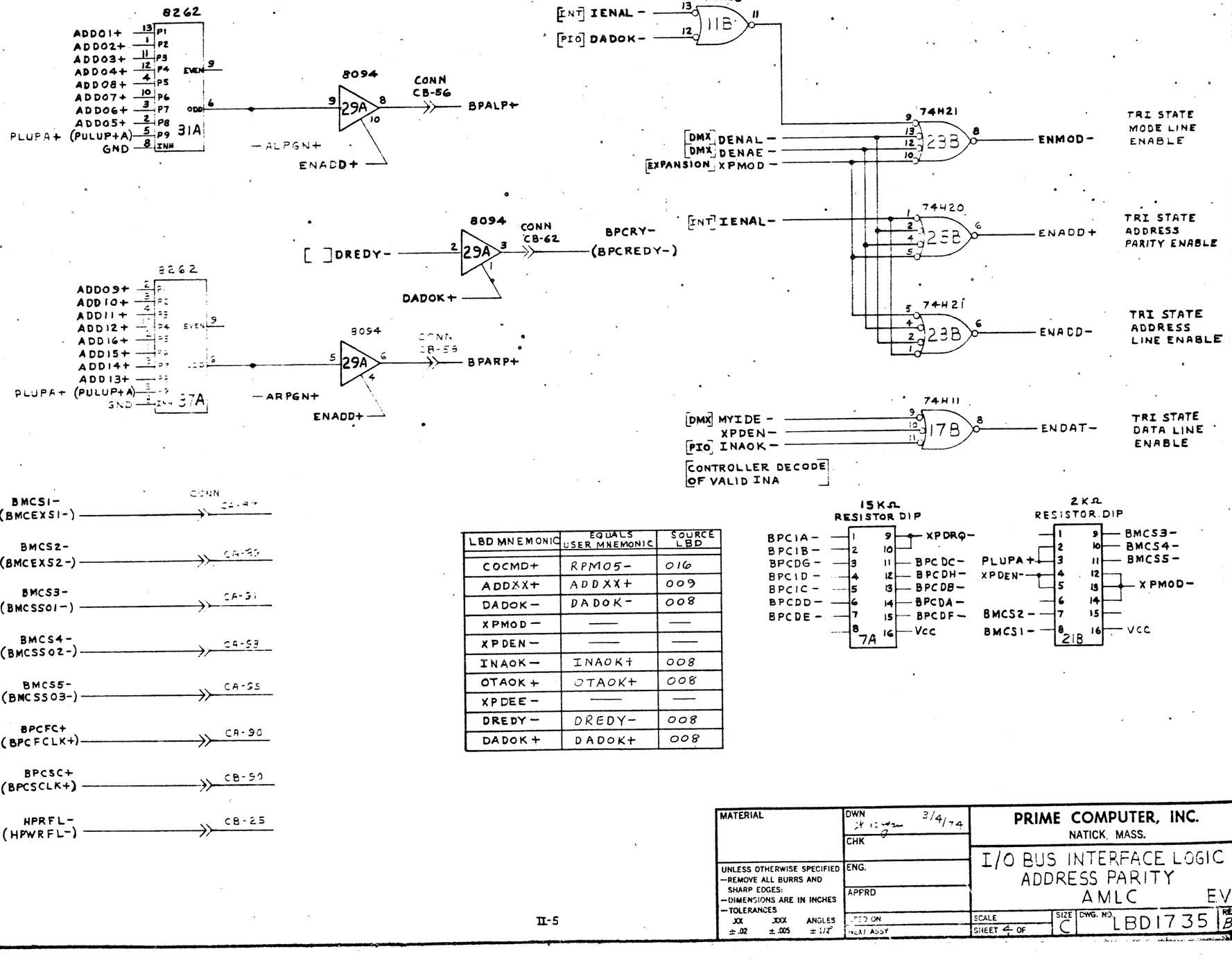
FUNCTION DECODERS



OCTAL ADDRESS DECODERS

MATERIAL	DWN Jr Bogan 3/14/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	I/O BUS INTERFACE LOGIC ADDRESS DECODING AMLC EV
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 3 OF — SIZE C — DWG. NO. LBD1735 — REV. A

PDF-003



BMCS1- (BMCEXS1-) → CONN CA-87

BMCS2- (BMCEXS2-) → CA-89

BMCS3- (BMCSS01-) → CA-91

BMCS4- (BMCSS02-) → CA-93

BMCS5- (BMCSS03-) → CA-95

BPCFC+ (BPCFCLK+) → CA-90

BPCSC+ (BPCSCLK+) → CB-90

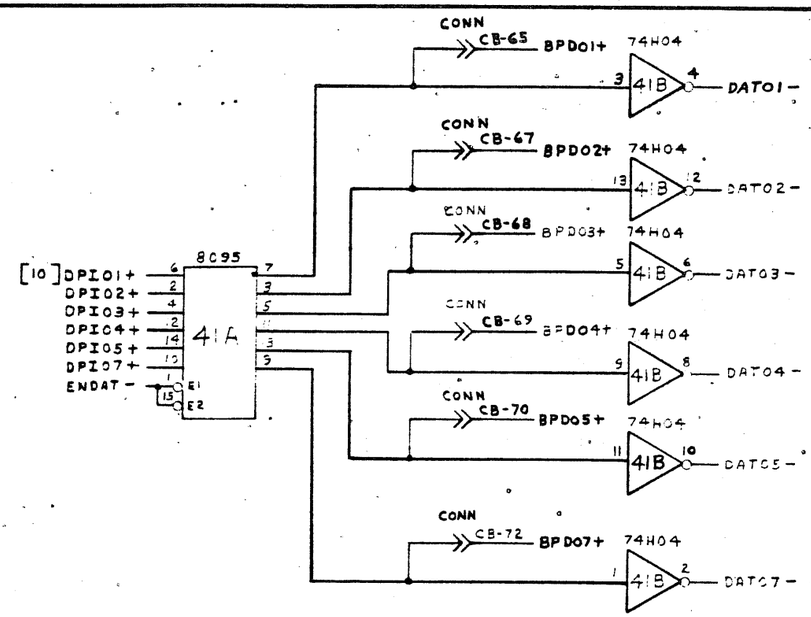
HPRFL- (HPWRFL-) → CB-25

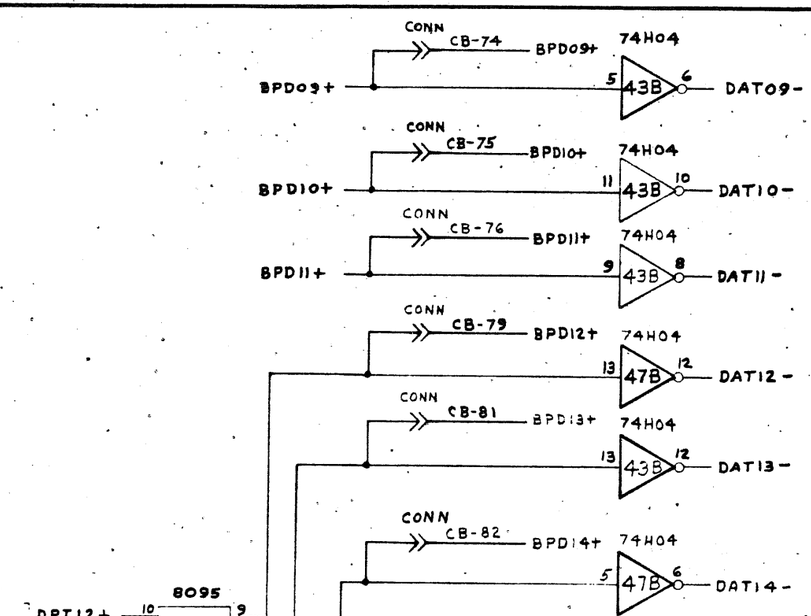
LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
COCMD+	RPM05-	016
ADDXX+	ADDXX+	009
DADOK-	DADOK-	008
XPMOD-	——	——
XPDEN-	——	——
INAOK-	INAOK+	008
OTAOK+	OTAOK+	008
XPDEE-	——	——
DREDY-	DREDY-	008
DADOK+	DADOK+	008

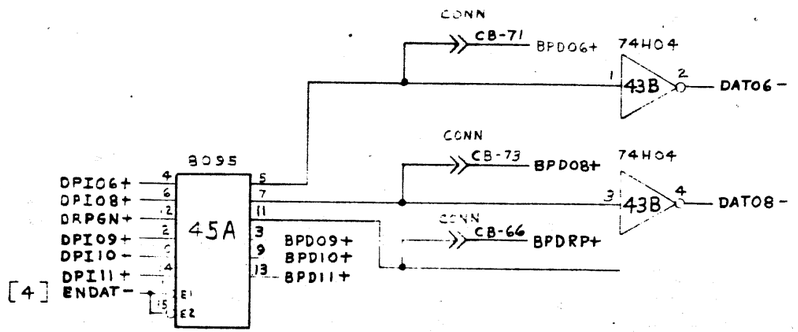
MATERIAL	DWN 3/4/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	I/O BUS INTERFACE LOGIC ADDRESS PARITY AMLC EV
	ENG.	
	APPRD	
	PROD ON NEXT ASSY	SCALE SHEET 4 OF
		SIZE C DWG. NO. LBD1735 REV. B

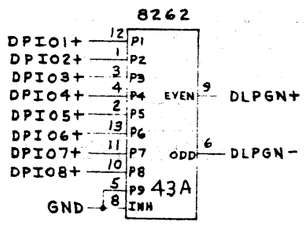
PDF-003

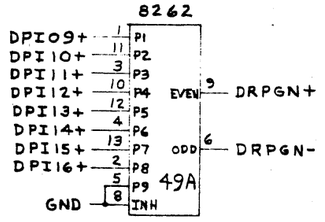
PRIME COMPUTER, INC.











LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
DPIXX+	DPIXX+	010

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	I/O BUS INTERFACE LOGIC DATA BUS LINES AMLC EV
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 5 OF
		SIZE C
		DWG. NO. LBD1735
		REV. A

PDF-003

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

74H53 13B
ISHIC-
HPAIF+
ISPRQ+
IPNRQ+
ISHIC-
ICPNP-
IXPIP-
IXPIP+

VCC
R99
PLUPB+

CONN
BPC1A-(BPCIPNA-) CA-18
BPC1B-(BPCIPNB-) CA-19
BPC1C-(BPCIPNC-) CA-20
BPC1D-(BPCIPND-) CA-21
74H20 9A
IPNOR-
BPCIPND- ENDS IN THIS CONTROLLER

74H04 11A
IPNOR+

CONN CA-17 BPC1O- (BPCIPNO-)

IPNOR+
IRQOR+
HPAIF-
74H10 19A
GIRQO-
74H00 21A
CTIRQ+
74H01 23A
OPEN COLLECTOR
CONN CA-92 BPCIR- (BPCIRQ-)

IENAL+
ISPRQ+
74H10 19B
KCNSI-
USED TO COUNT OVERRIDE INHIBIT INTERRUPT CYCLES IN THE CONTROLLER IF NEEDED

IENAP-
74H10 19A
GCNIR-
IPNRQ-
74H10 19A

BPCOV- (BPCIOVI-) CONN CA-38
74H04 11A
IENAP+
ISHIP+
74H00 7B
ISHIC-

CONTROLLER NORMAL INTERRUPT REQUEST

74H00 21A
XGIRQ-

BPCIN+ (BPCIEN+) CONN CA-16
74H04 11A
IENAP-
74H04 11A
IENAP+

PLUPB+
CNIRQ+
KIPNR-
74H74 13A
IPNRQ+
IPNRQ-

ISPRQ+
IPNRQ+
IENAL+
74H10 19B
CMYIN-
USED TO COUNT NORMAL INTERRUPT CYCLES IN THE CONTROLLER IF NEEDED

BPCPN+ (BPCICPN+) CONN CA-23
74H04 11A
CINIA- (CINIT-A)
74H09 11B
ICPNP-

PLUPB+
CNSIR+
IENAP+
74H74 13A
ISPRQ+
ISPRQ-

ISPRQ-
74H00 21A
XGIRQ+
74H00 21A
74H01 23A
OPEN COLLECTOR
CONN CA-38 BPCOV- (BPCIOVI-)

X1
X2
21A (GND)

CONTROLLER OVERRIDE INHIBIT INTERRUPT REQUEST
74H00 21A
GCNSI-

74H00 7B
SIENA-
SIENA+
74H106 5A
PLUPB+
IENAP+
GND
KIPNR-
IENAL+
IENAL-

PLUPB+ (PULUP+B)
IETCL+
IETCL-
74H74 15B

PLUPB+ (PULUP+B)
IPNOR+
IENAP+
74H74 15B
KHPAI+
KHPAI-
HPAIF+

IPNOR+
ISHIC-
IPNRQ+
74H11 17B
LHPAI+

CINIA- (CINIT-A)
74H11 17B
KHPAF-

PLUPB+ (PULUP+B)
IENAP+
GND
74H106 15A
HPAIF+
HPAIF-

74H55 7A
ISPRQ+
ISHIP+
IPNOR+
IPNRQ+
ISHIC-

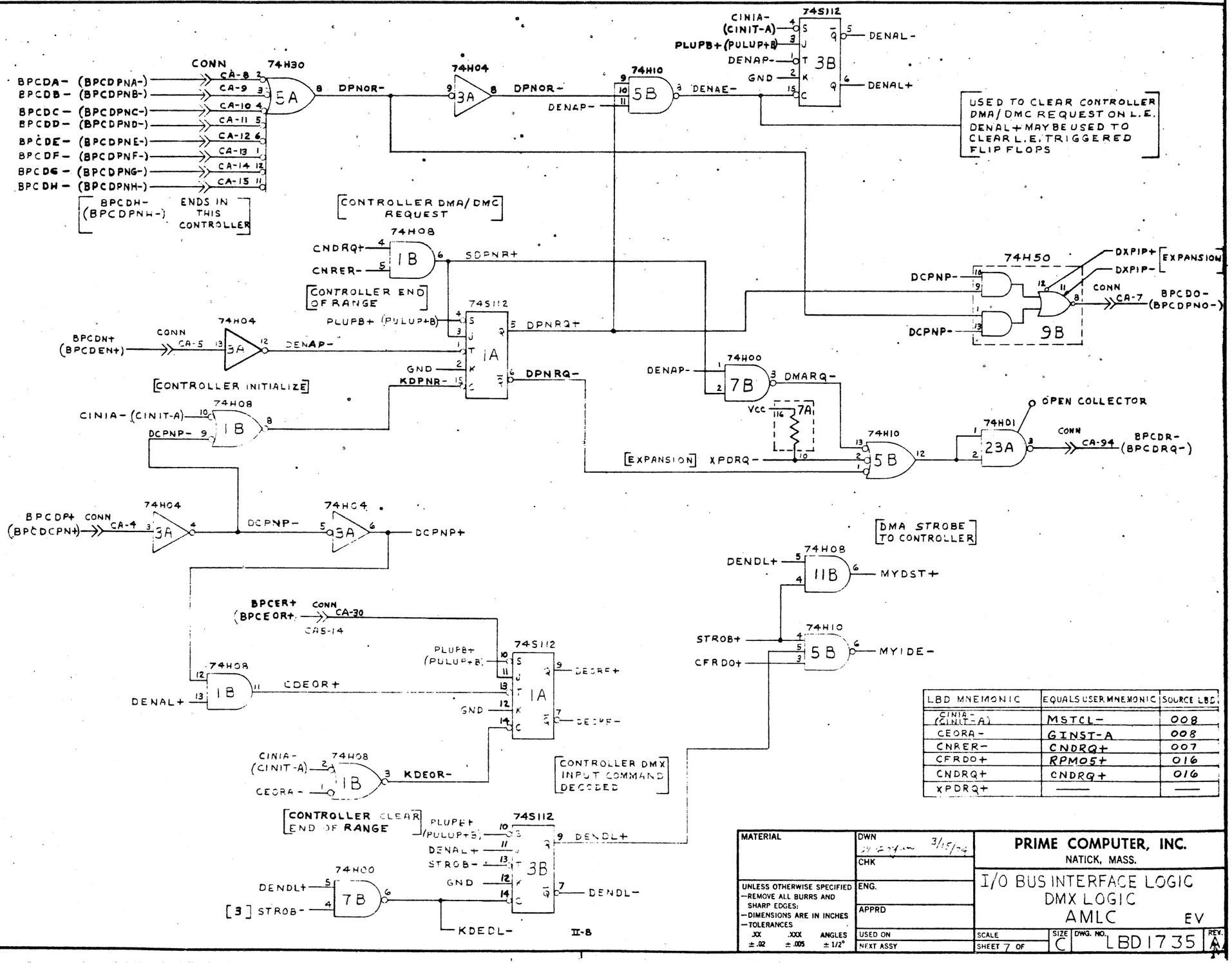
74H04 11A
HPAIF+

BPCHI+ (BPCCHI+) CONN CA-25

NOTE
1. PRIME INTERRUPT LOGIC WITH OVERRIDE INHIBIT INTERRUPT.
2. CUTX1 TO EXPAND INTERRUPT REQUESTS.
3. CUTX2 TO IMPLEMENT OVERRIDE INHIBIT INTERRUPTS

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	I/O BUS INTERFACE LOGIC CONTROLLER INTERRUPT AMLC EV
	APPRD	
	USED ON	SCALE
	NEXT ASSY	SHEET 6 OF
		SIZE C DWG. NO. LBD1735 REV A

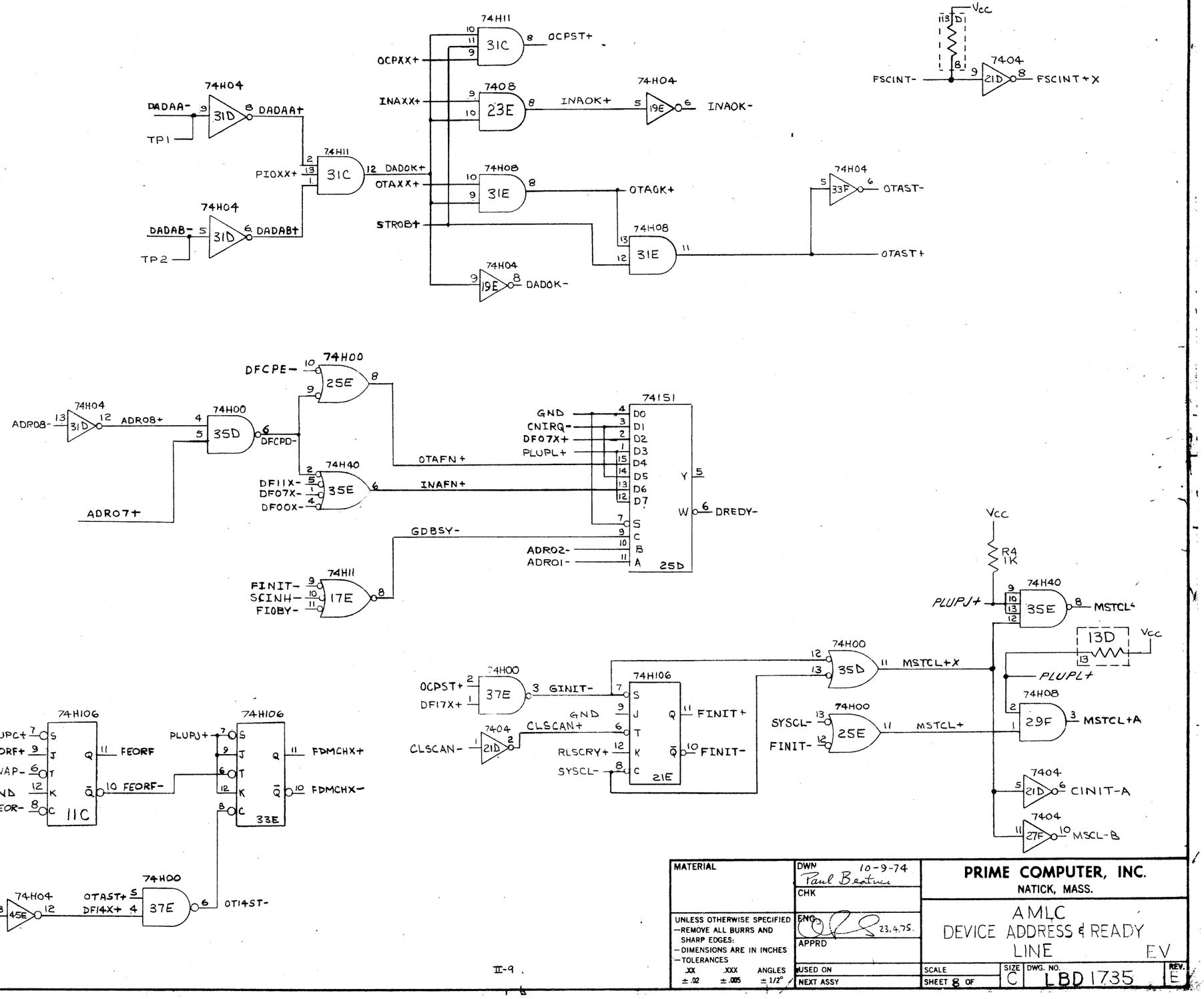
PDF-003



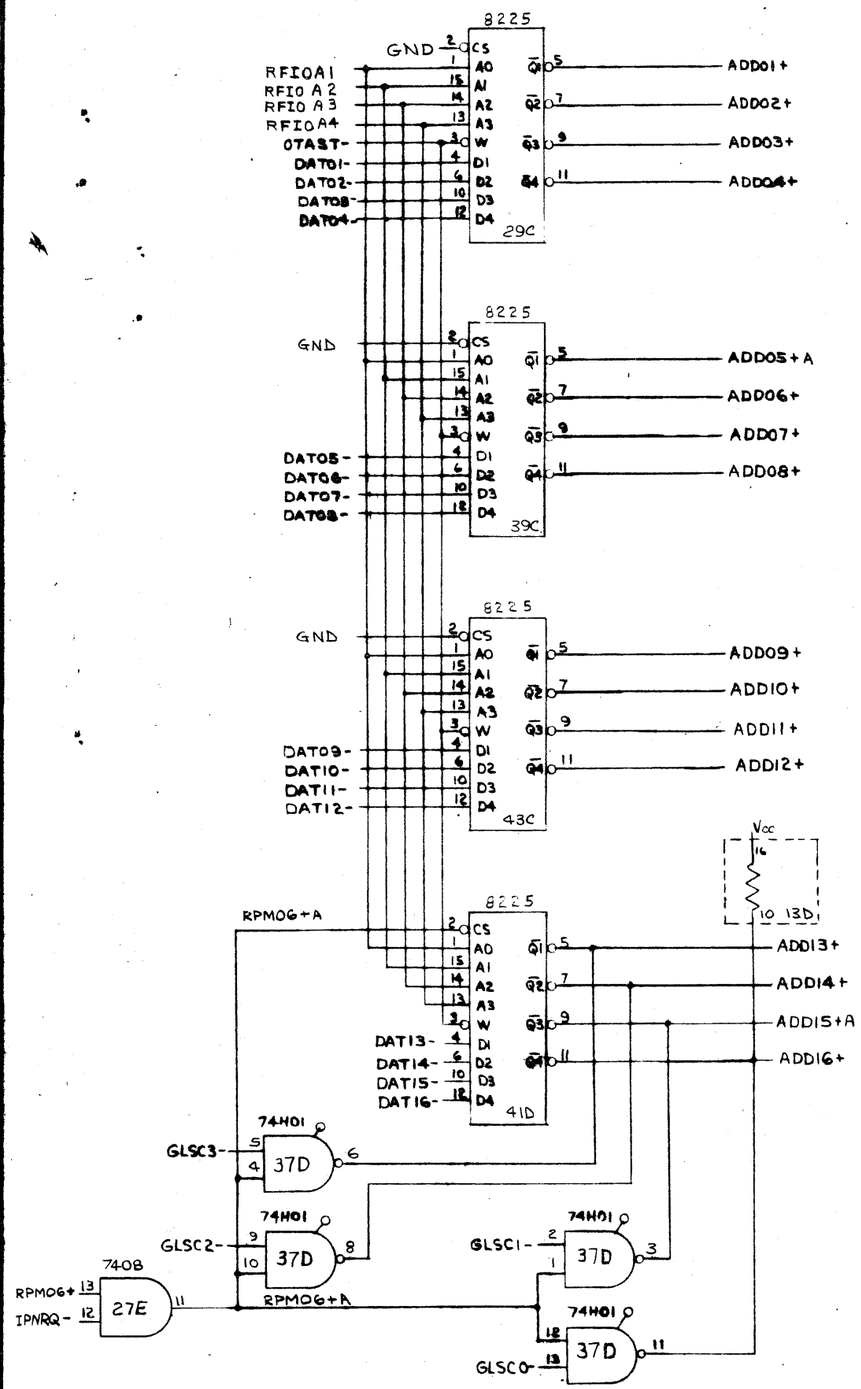
LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
CINIA- (CINIT-A)	MSTCL-	008
CEORA-	GINST-A	008
CNRER-	CNDRQ+	007
CFRDO+	RPM05+	016
CNDRQ+	CNDRQ+	016
XPDRQ+	——	——

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	I/O BUS INTERFACE LOGIC DMX LOGIC AMLC EV
	APPRD	
	USED ON	SCALE
	NEXT ASSY	SHEET 7 OF
		SIZE C DWG. NO. LBD1735 REV. A

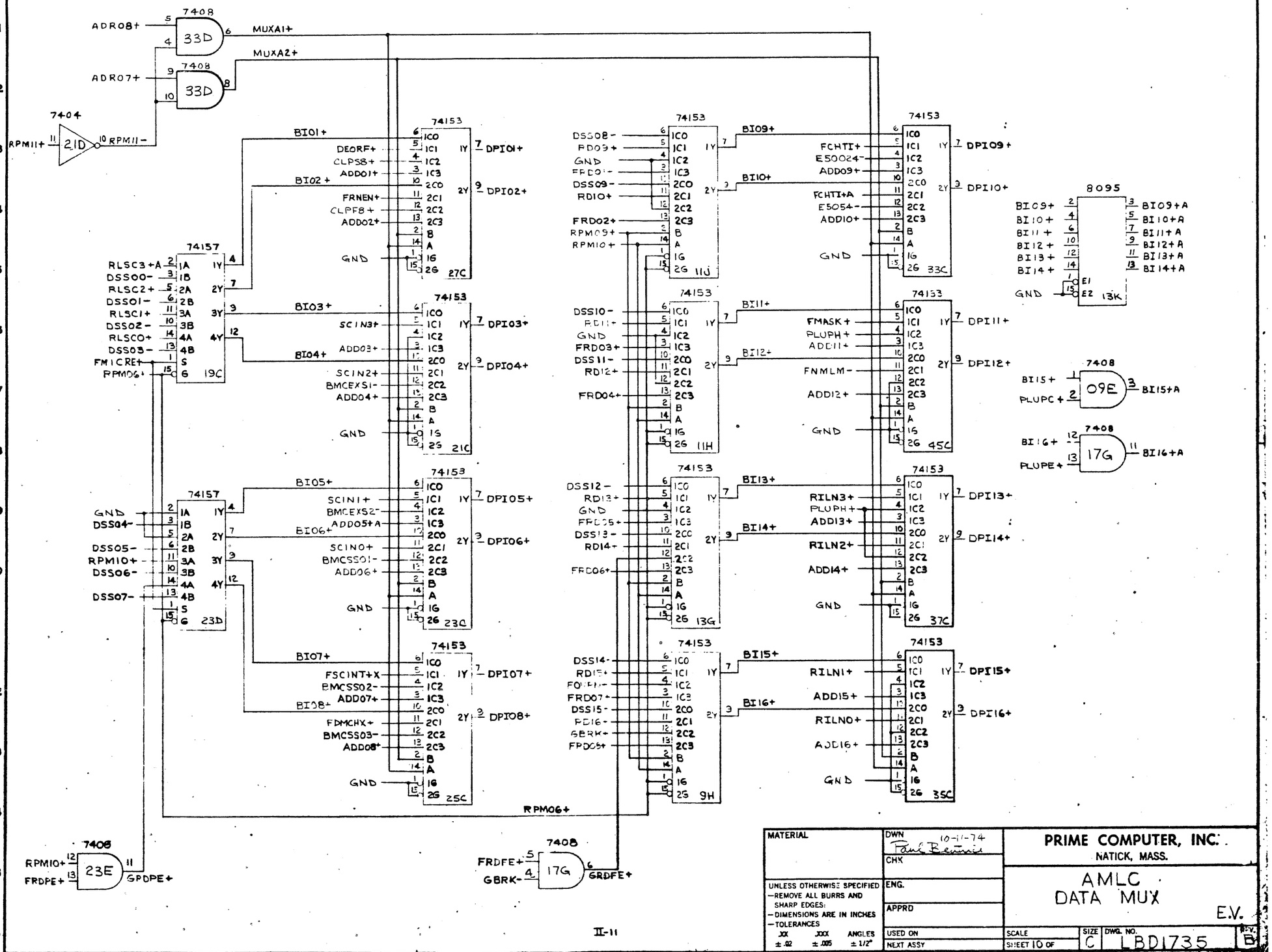
PDF-003



MATERIAL	DWN 10-9-74 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG 23,4,75.	AMLC DEVICE ADDRESS & READY LINE	
	APPRD		
	USED ON NEXT ASSY	SCALE SHEET 8 OF	SIZE C DWG. NO. LBD1735 REV. E

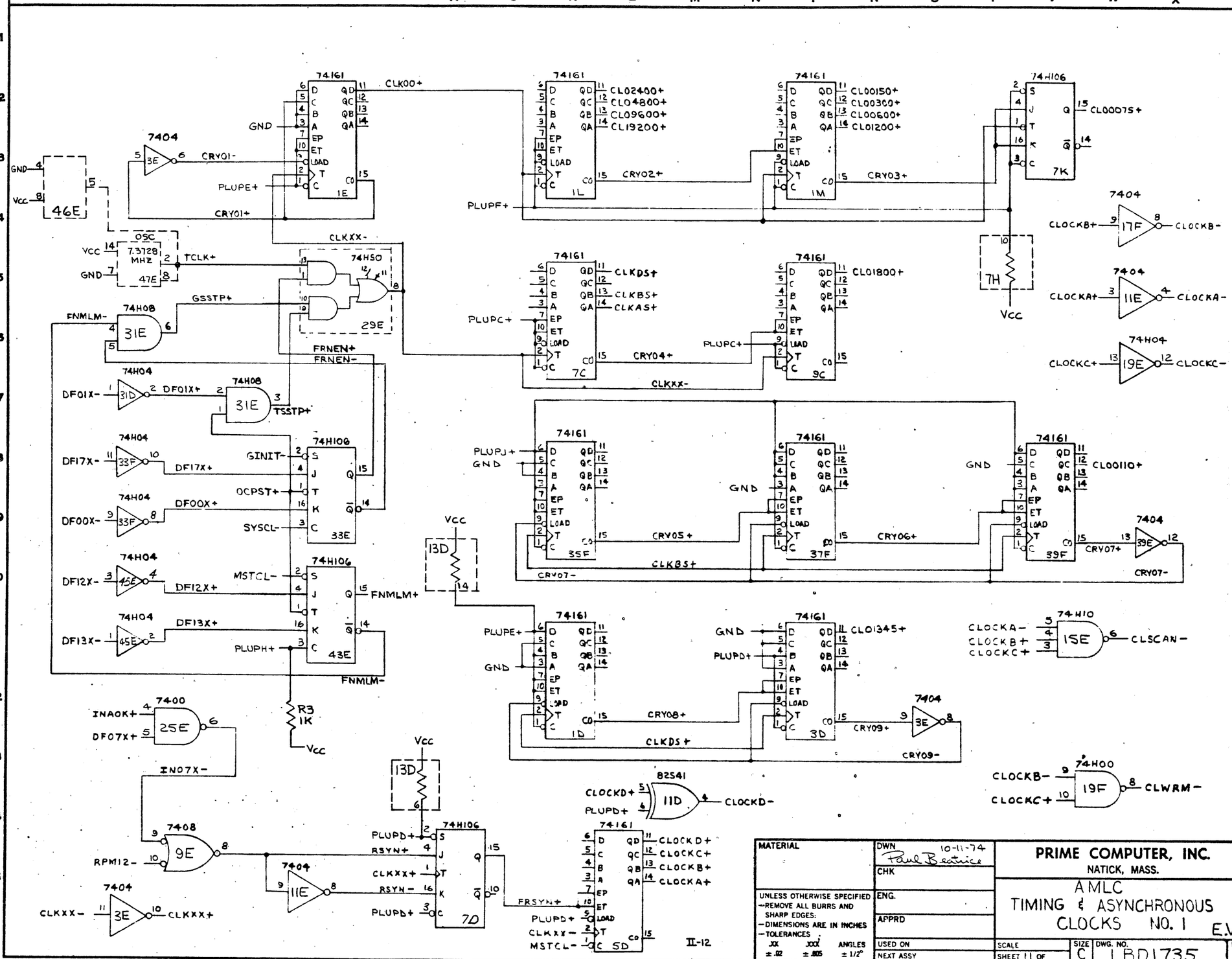


MATERIAL	DWN 10/9/74 Paul Beatie	PRIME COMPUTER, INC.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: — DIMENSIONS ARE IN INCHES — TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ± 1/2°	ENG.	AMLC ADDRESS & DATA REGISTERS
	APPRD	
	USED ON	SCALE
	NEXT ASSY	SIZE C DWG. NO. BD 1735 REV B

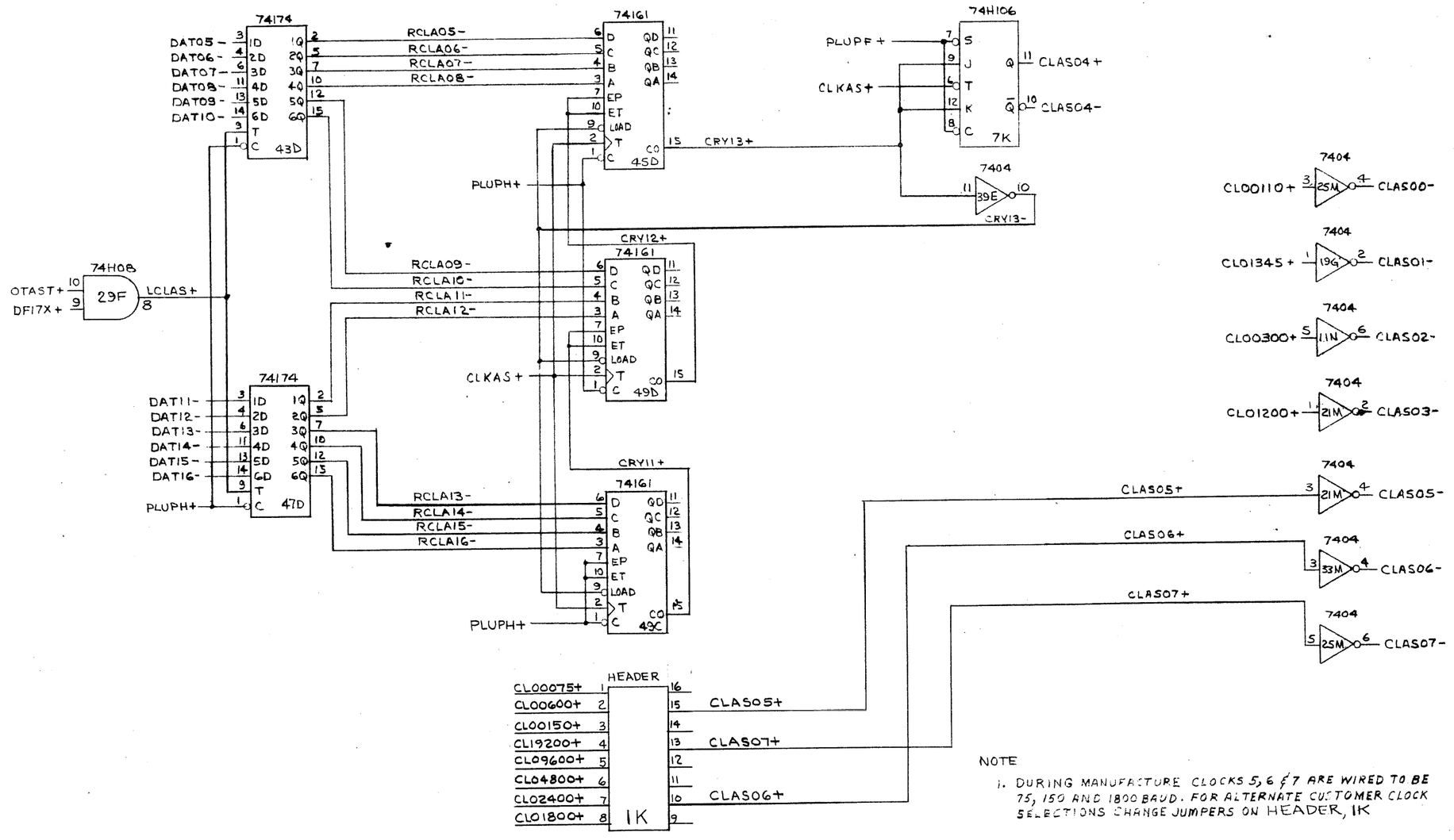


MATERIAL	DWN 10-11-74 Paul Bennis	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: — DIMENSIONS ARE IN INCHES — TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	AMLC DATA MUX E.V.
	APPRD	
USED ON	SCALE	SIZE C DWG. NO. LBD1735 REV. B
NEXT ASSY	SHEET 10 OF	

PRIME COMPUTER, INC.



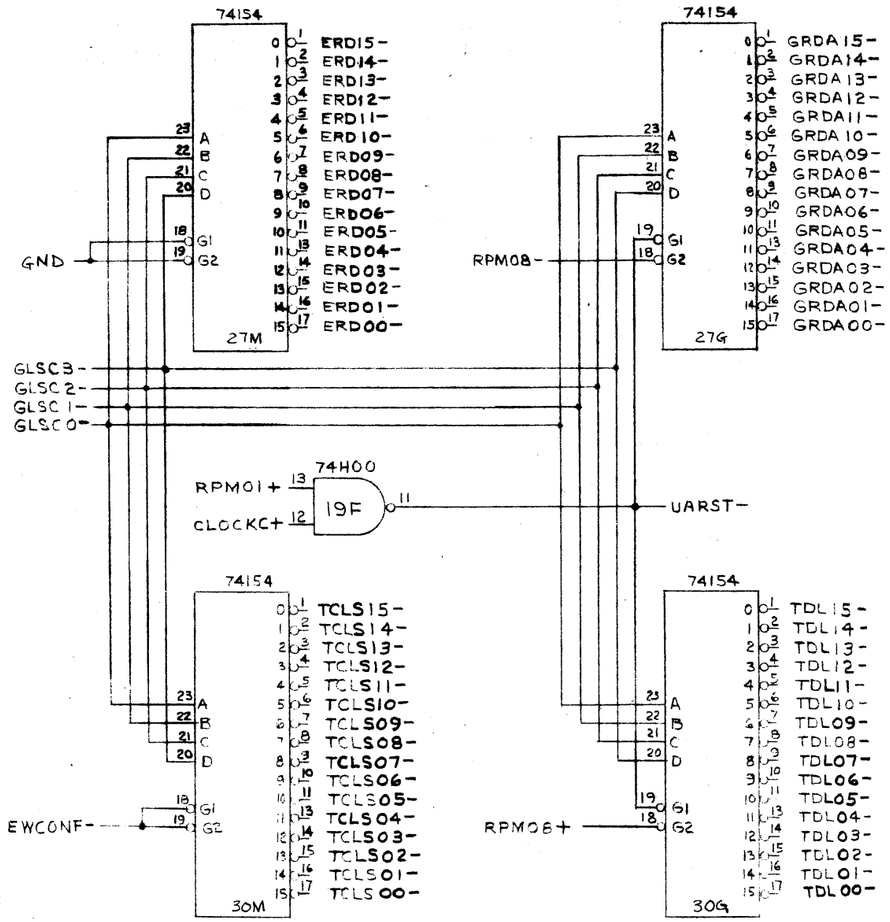
MATERIAL	DWN 10-11-74 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK	AMLC TIMING & ASYNCHRONOUS CLOCKS NO. 1	E.V.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.		
	APPRD		
	USED ON	SCALE	SIZE C DWG. NO. LBD1735 REV. E
	NEXT ASSY	SHEET 11 OF	

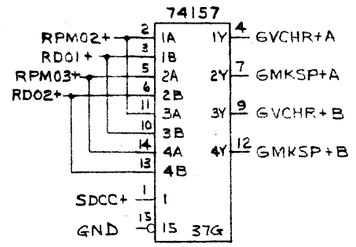


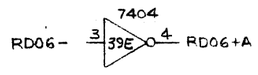
NOTE

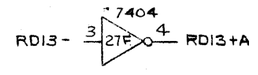
1. DURING MANUFACTURE CLOCKS 5, 6 & 7 ARE WIRED TO BE 75, 150 AND 1800 BAUD. FOR ALTERNATE CUSTOMER CLOCK SELECTIONS CHANGE JUMPERS ON HEADER, 1K

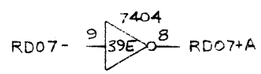
MATERIAL	DWN 10-9-74 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	AMLC TIMING 2, ASYNCHONOUS CLK NO.2 (CUSTOMER OPTIONS) E.V.
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 12 OF
		SIZE C / DWG. NO. LBD1735 / REV. B

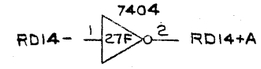


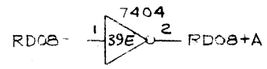


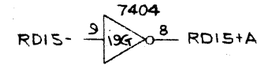


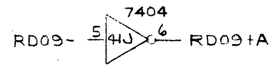


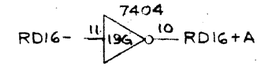


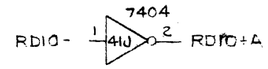


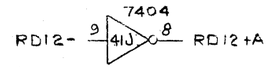


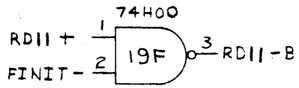




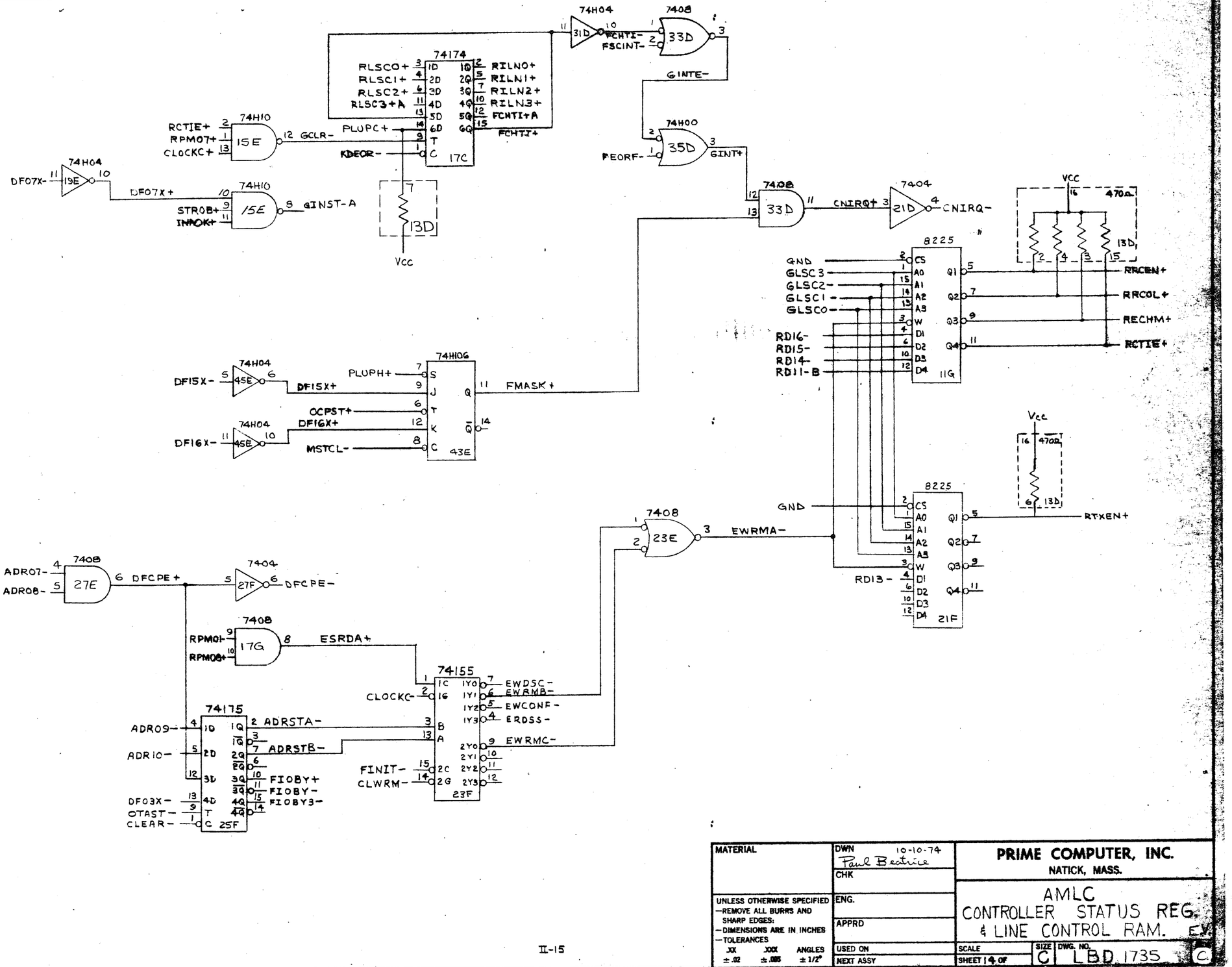








MATERIAL	DWN 10-10-74 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	AMLC LINE CONTROL-MULTIPLEXER & SIGNAL BUFFERING E.V.
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 13 OF / SIZE C / DWG. NO. LBD1735 / REV. B



MATERIAL	DWN 10-10-74 Paul Bertrice	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	CHK	AMLC CONTROLLER STATUS REG. & LINE CONTROL RAM.
	ENG.	
	APPRD	
USED ON / NEXT ASSY	SCALE / SHEET 14 OF	SIZE C / DWG. NO. LBD 1735 / C

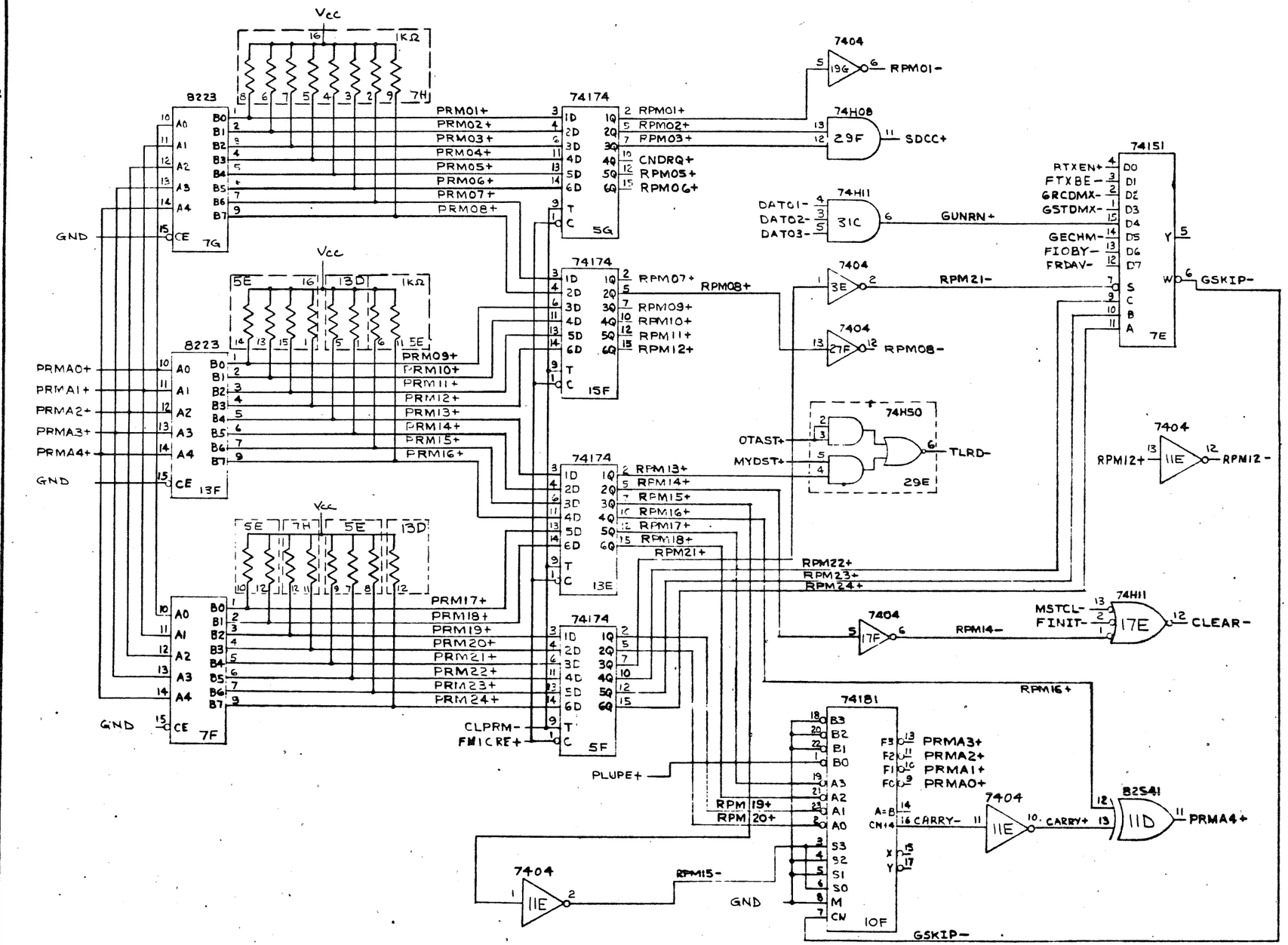
PDF-003

74H00 19F
74H08 17G
74174 15G
74175 13J
74175 15H
74175 15C
74H04 19E
7404 17F
7404 17F
74H11 17E
82S26 9G
74161 17D
74158 19D
74157 27D
74157 47C
74H30 13H
74H106 21E
7410 9D
7408 23E
74H00 25E
74H00 35D
7404 3E
7404 1G
7404 19G
7404 21D
7404 39E
82S41 11D
74153 15C
1KΩ 7H
1KΩ 13D

BTXBE+ GTXEN+ STXBE+ RTXEN- RTXEN+ RCTIE- RCTIE+
BRDAV+ BRDPE+ BRDFE+ BOVRN+ FRDAV+ FRDPE+ FRDFE+ FOVRN+ FTXBE+ FRDAV- FTXBE-
BRD01+ BRD02+ BRD03+ BRD04+ CLEAR- FRD01+ FRD02+ FRD03+ FRD04+ FRD01- FRD02- FRD03- FRD04-
BRD05+ BRD06+ BRD07+ BRD08+ CLSTC- FRD05+ FRD06+ FRD07+ FRD08+ FRD05- FRD06- FRD07- FRD08-
RRCEN+ RRCOL+ RECHM+ GND GCHZR- GRCDMX+ GSTDMX+ GBRK+ GECHM+ GRCDMX- GSTDMX- GBRK- GECHM-
CLWRM+ FMICRE- CLOCKD- MSTCL-
SMICE+A DADOK- SMICE+ FIOBY- SCINH-
PLUPD+ CLOCKC+ RPM14+ FMICRE- FMICRE+
CLOCKC+ DENAE- GND MYDST+ RLSC3+ RPM11+ RPM12+ GND E5054- CLPRM+ RLSC3+A CLPRM-
VCC
RPM06+ RPM06-
ADD05+A ADD05-
GMDG+ RPM06-
CLOCKD+ PLUPC+ CLSCAN- MSTCL- RLSCRY+
RLSC3+ RLSC2+ RLSC1+ RLSCO+ RLSC3+A RD01+ RD02+ RD03+ RD04+ ESRDA+ GND GLSC3- GLSC2- GLSC1- GLSCO-
ADR07- ADR08- GND ADR09- PLUPL+ ADR10- RFIOA1- RFIOA2- RFIOA3-
IPNRQ+ RFIOA4-A RFIOA4-
INAXX+ RPM05+ GND PIOXX+ MODE0+ MODE1+ MODE2+ MODE4+

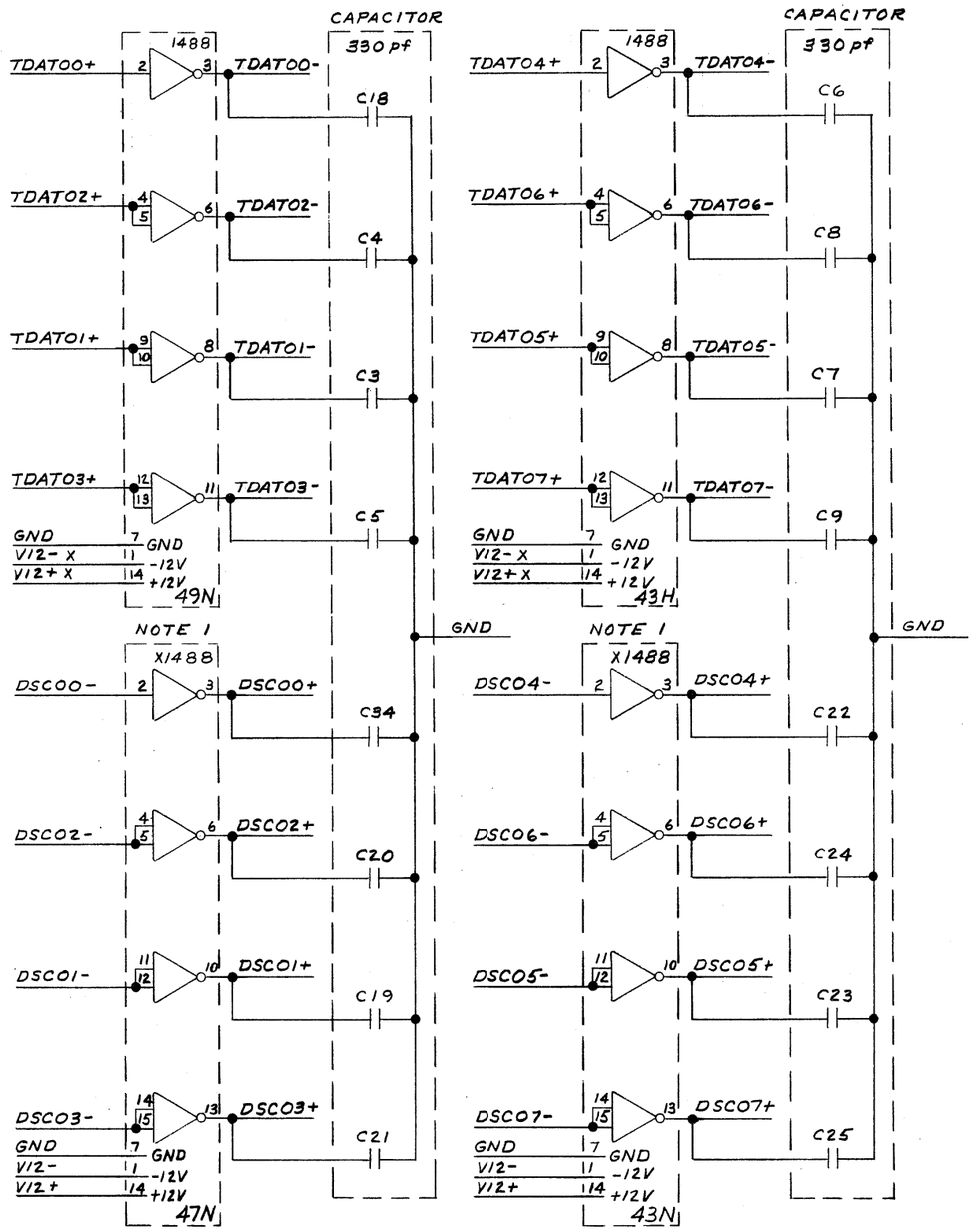
MATERIAL	DWN 10/10/74 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.03 XXX ±.005 ANGLES ±1/2°	CHK	AMLC MAIN CONTROL NO. 1
	ENG 23.4.75	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 15 OF
		SIZE C DWG. NO. LBD1735 REV. C

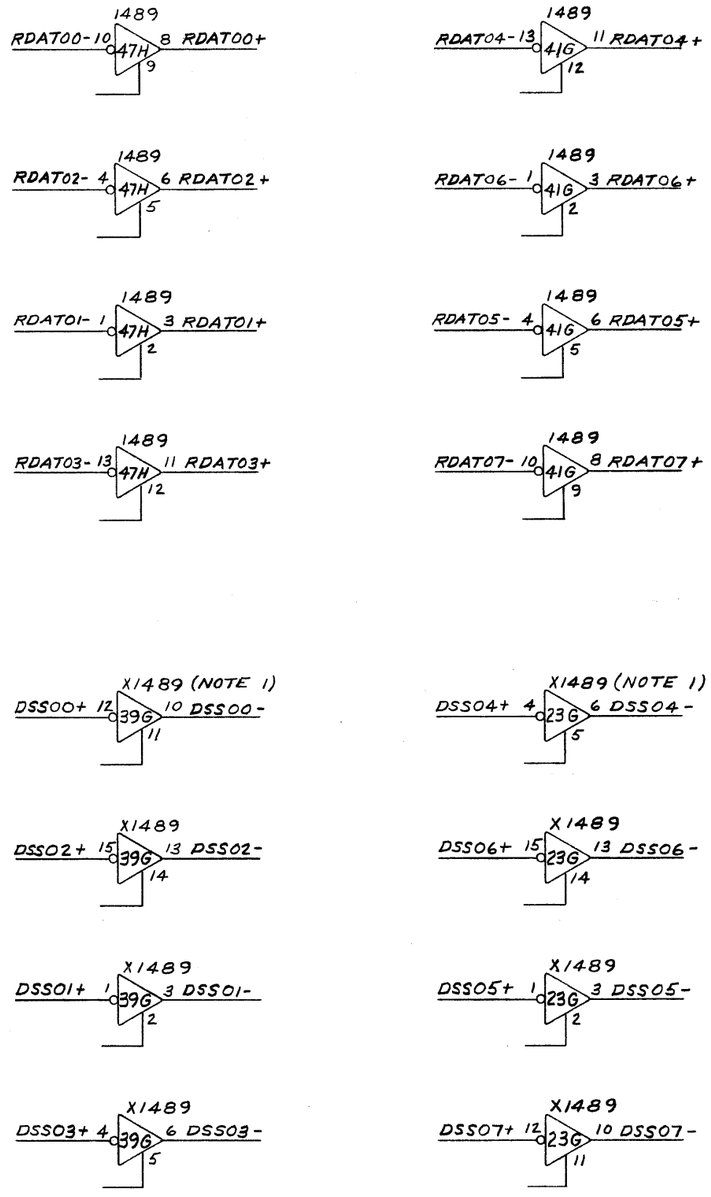
PDF-003



II-17

MATERIAL	DWN Paul Beatrice 10-11-74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ± .02 XXX ± .005 ANGLES ± 1/2°	CHK	AMLC MAIN CONTROL NO. 2 E.V.
	ENG.	
	APPRD	
USED ON	SCALE	SIZE C DWG. NO. LBD1735 REV. F
NEXT ASSY	SHEET 16 OF	





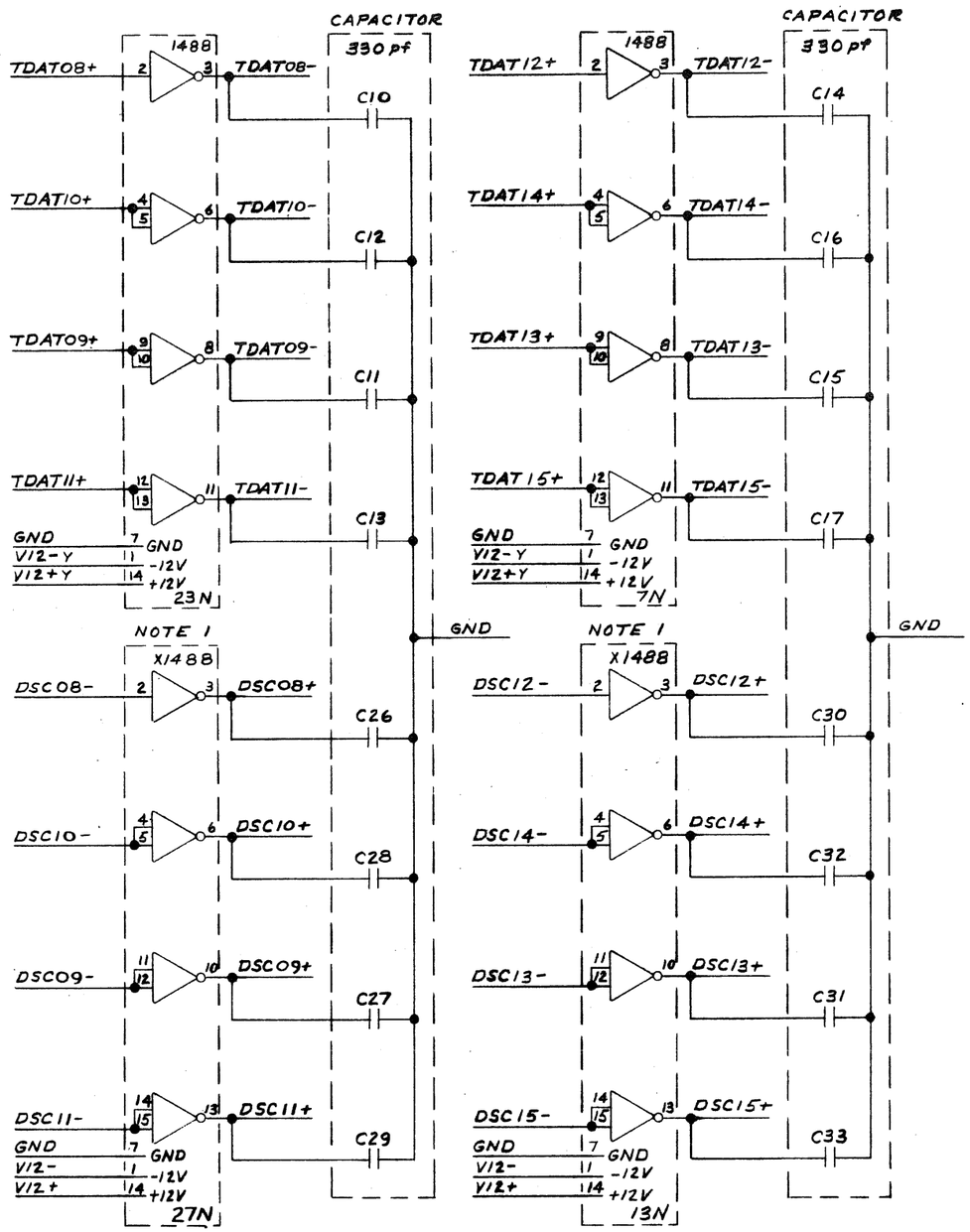
NOTE:
1. X1489 & X1488 DIPS ARE NOT PROVIDED ON AMLC MODELS 5002/5004

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

AMLC EIA INTERFACE
TX & RC DATA, MODEM
CONTROL & STATUS, LINES 0-7 EV

SHEET	SIZE	DWG. NO.	REV.
17 OF	C	LBD1735	D

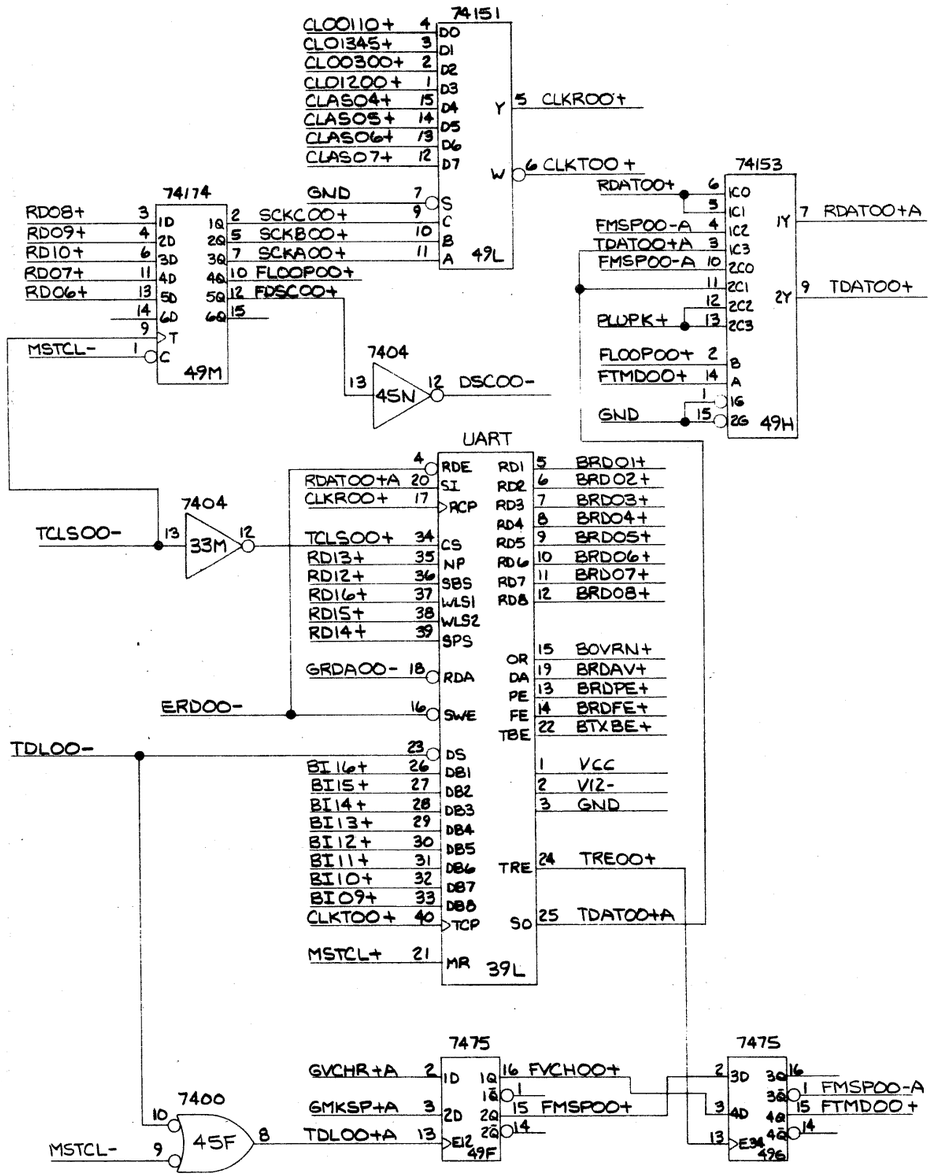
PDF-003



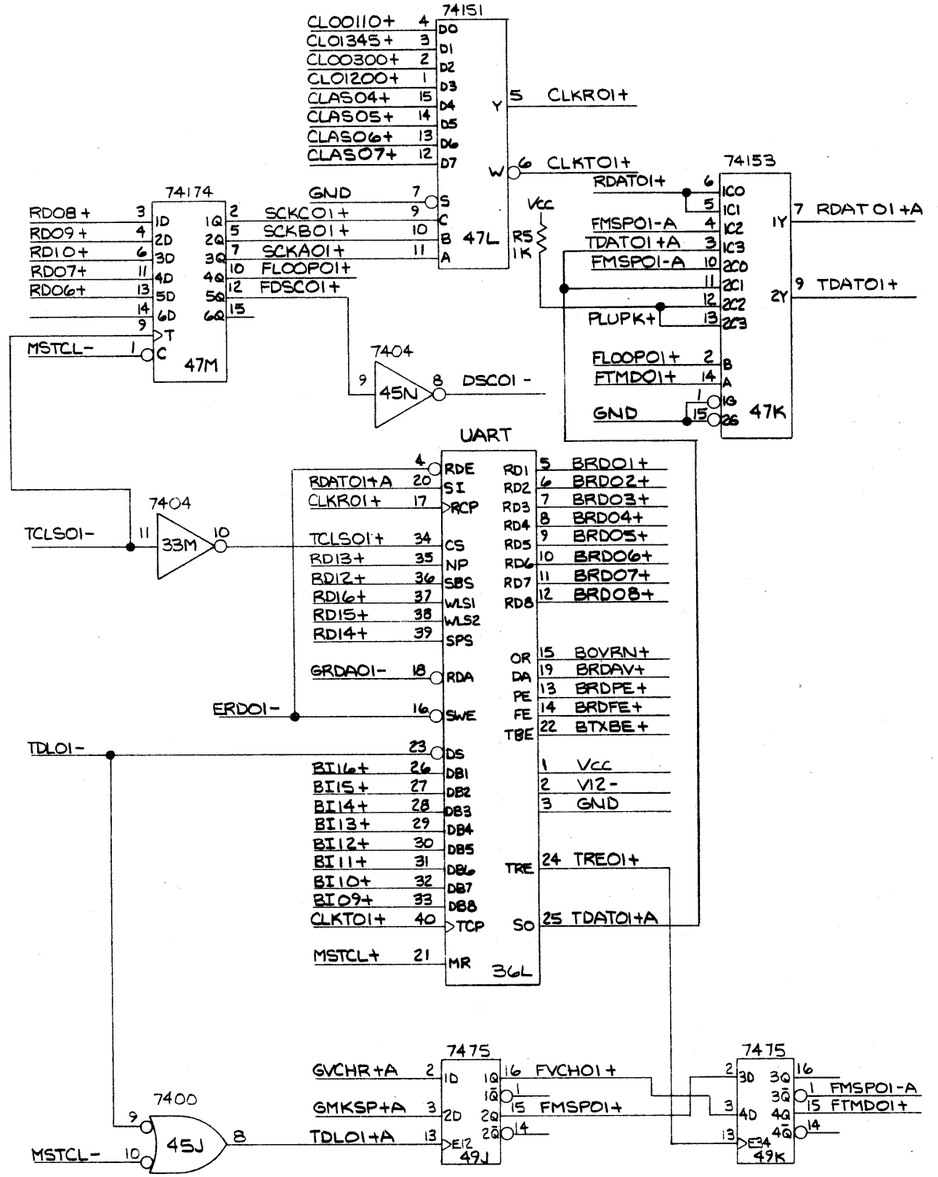
NOTE:
1. X1489 & X1488 DIPS ARE NOT PROVIDED ON AMLC MODELS 5002/5004

PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
AMLC EIA INTERFACE TX & RC DATA. MODEM CONTROL & STATUS. LINES 8-15 EV			
SHEET 18 OF	SIZE C	DWG. NO. LBD1735	REV. C

LINE #00



LINE #01

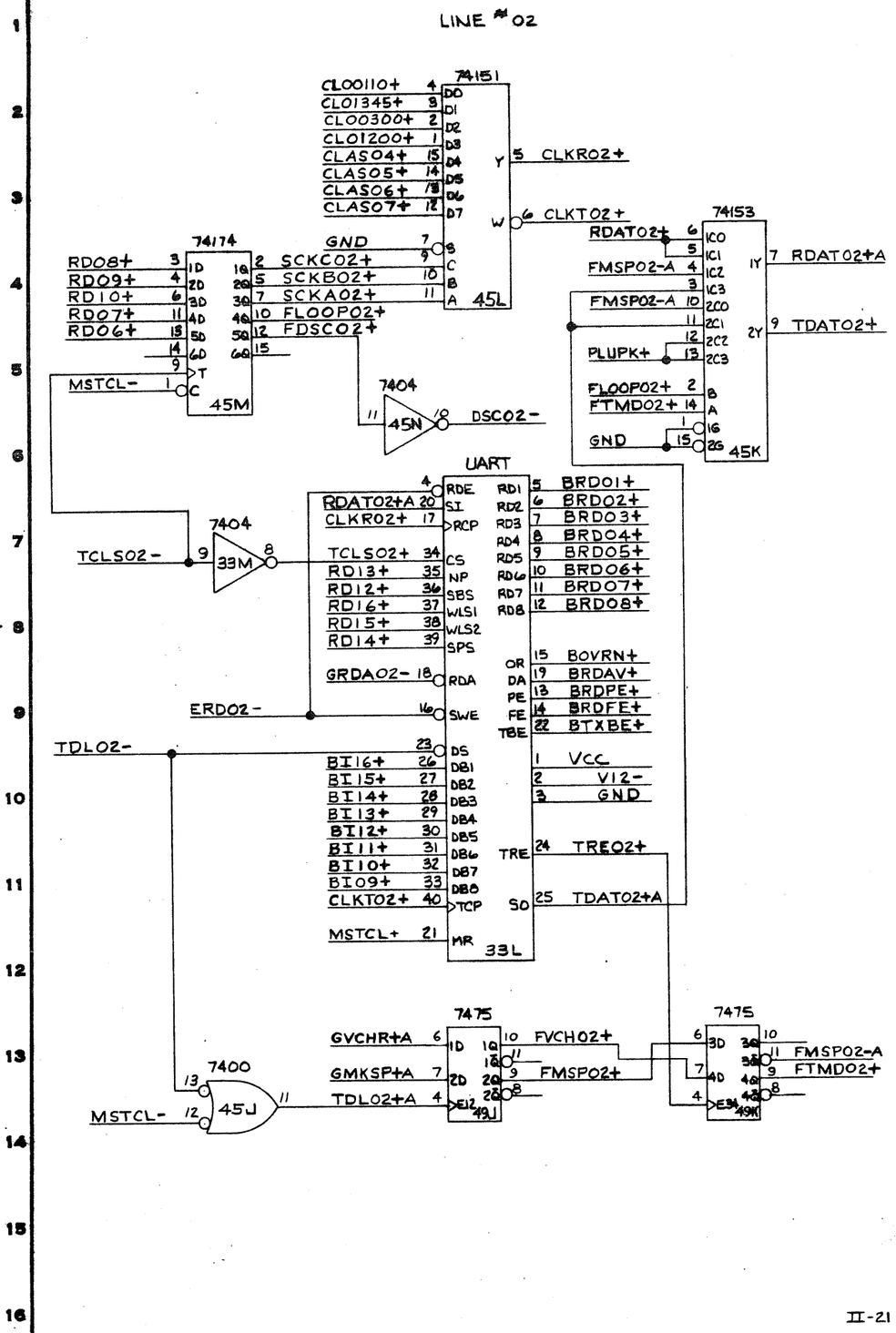


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

AMLC LINE INTERFACE
& CLOCK SELECT
(LINES 00 & 01) E.V

SHEET	OF	SIZE	DWG. NO.	REV.
19		C	LBD1735	C

PDF-003

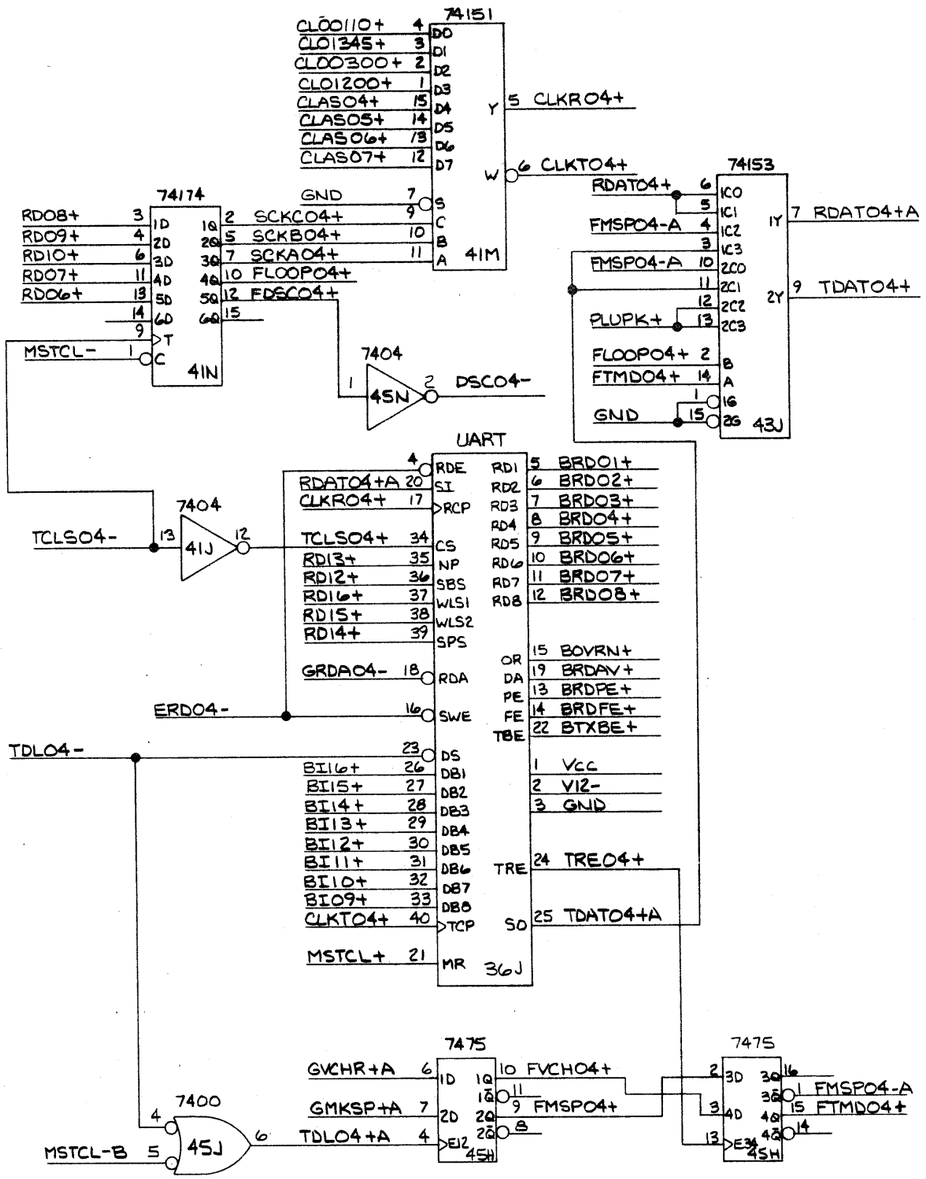


II-21

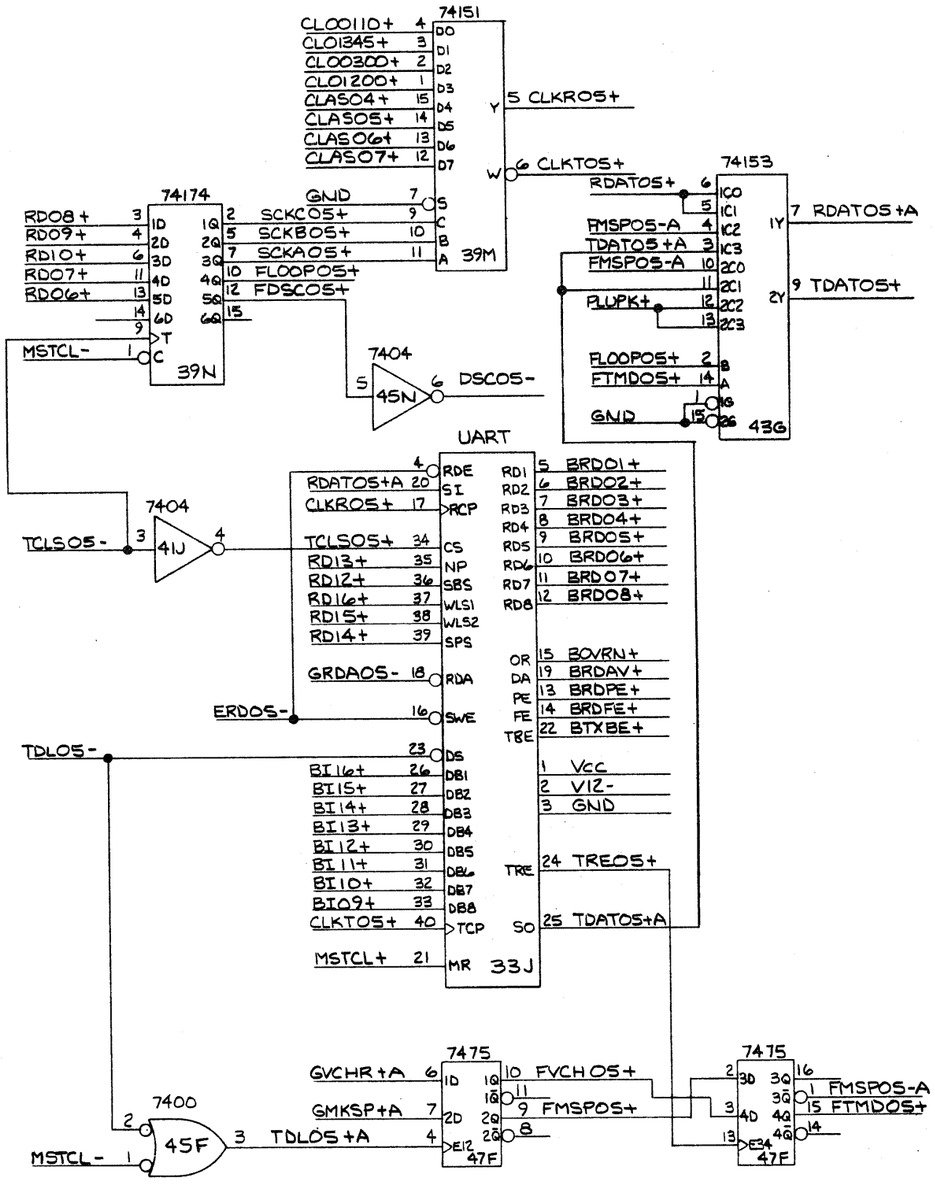
PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
AMLC LINE INTERFACE & CLOCK SELECT (LINES 02 & 03) E.V			
SHEET 20 OF	SIZE C	DWG. NO. LBD1735	REV. B

PDF-003

LINE # 04



LINE # 05

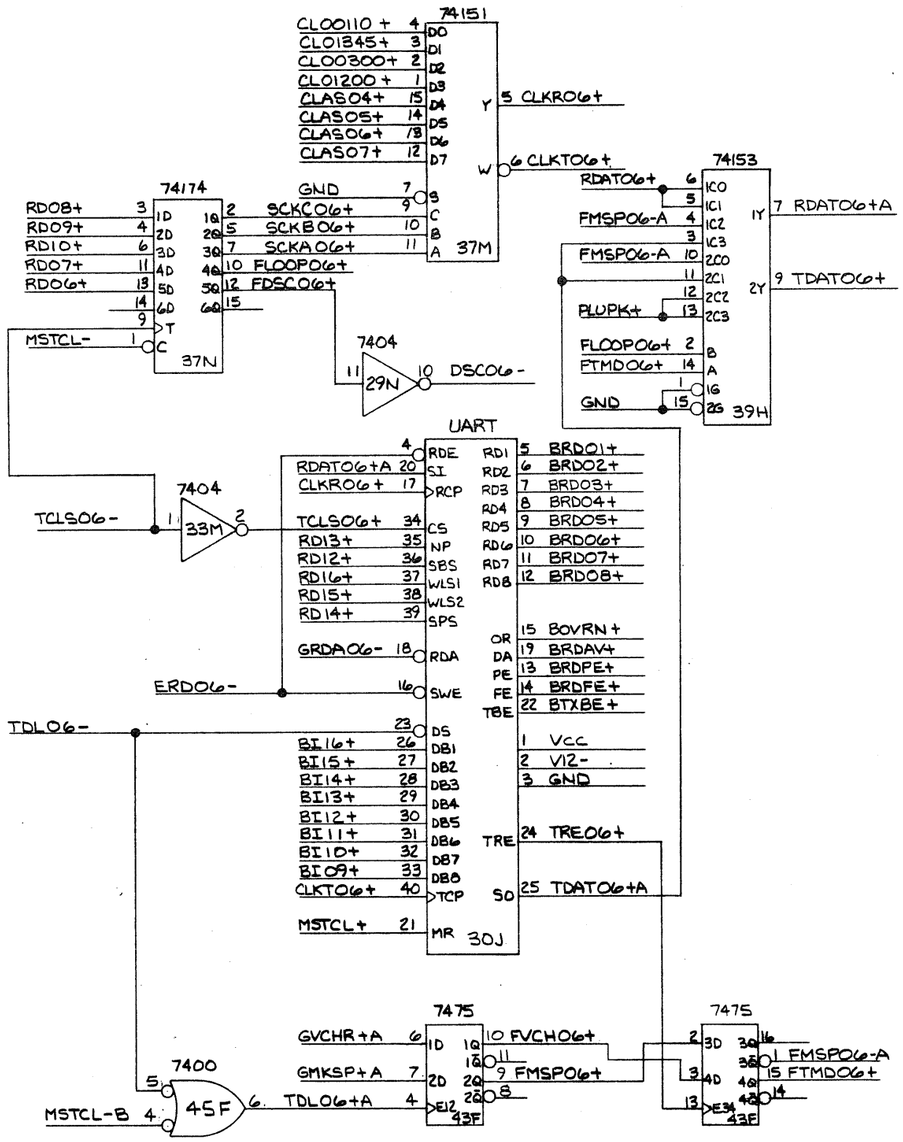


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

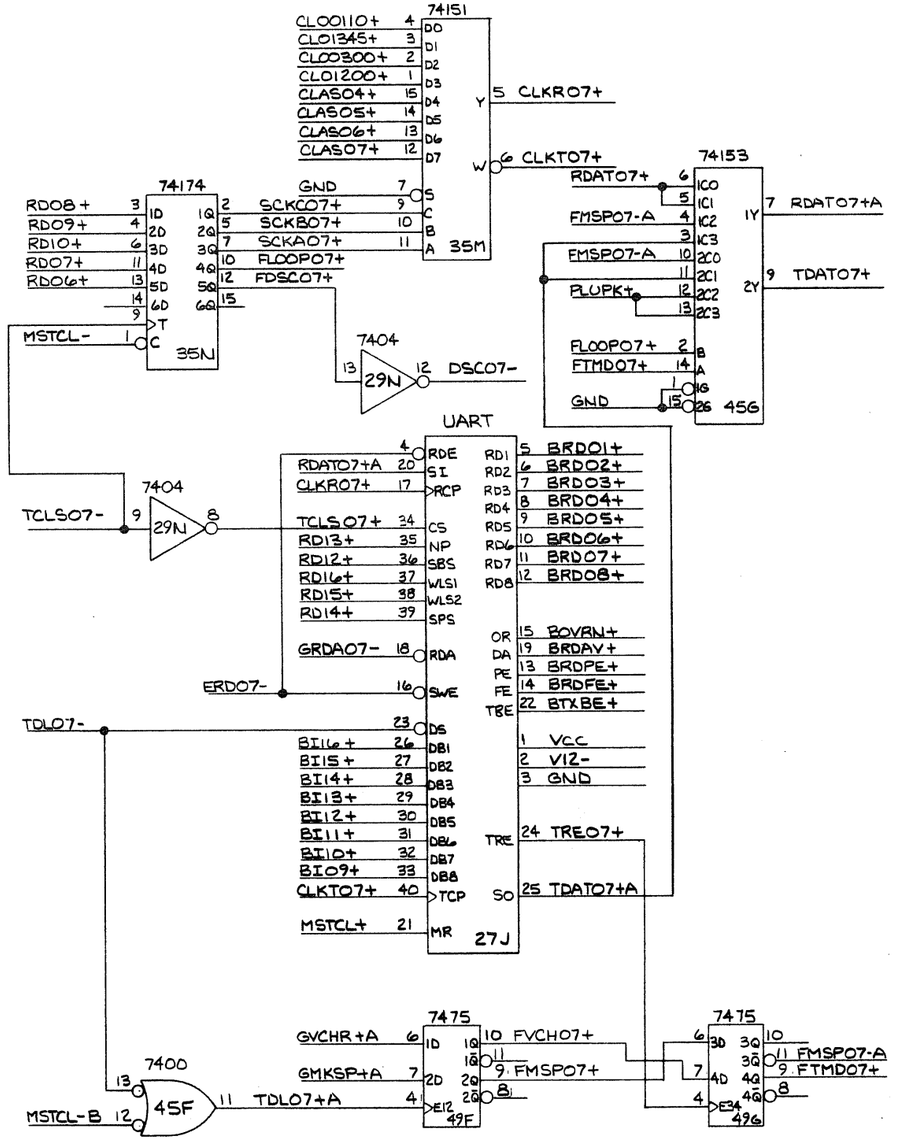
AMLC LINE INTERFACE
& CLOCK SELECT
(LINES 04 & 05) E.V

SHEET	SIZE	DWG. NO.	REV.
21 OF	C	LBD1735	C

LINE # 06



LINE # 07



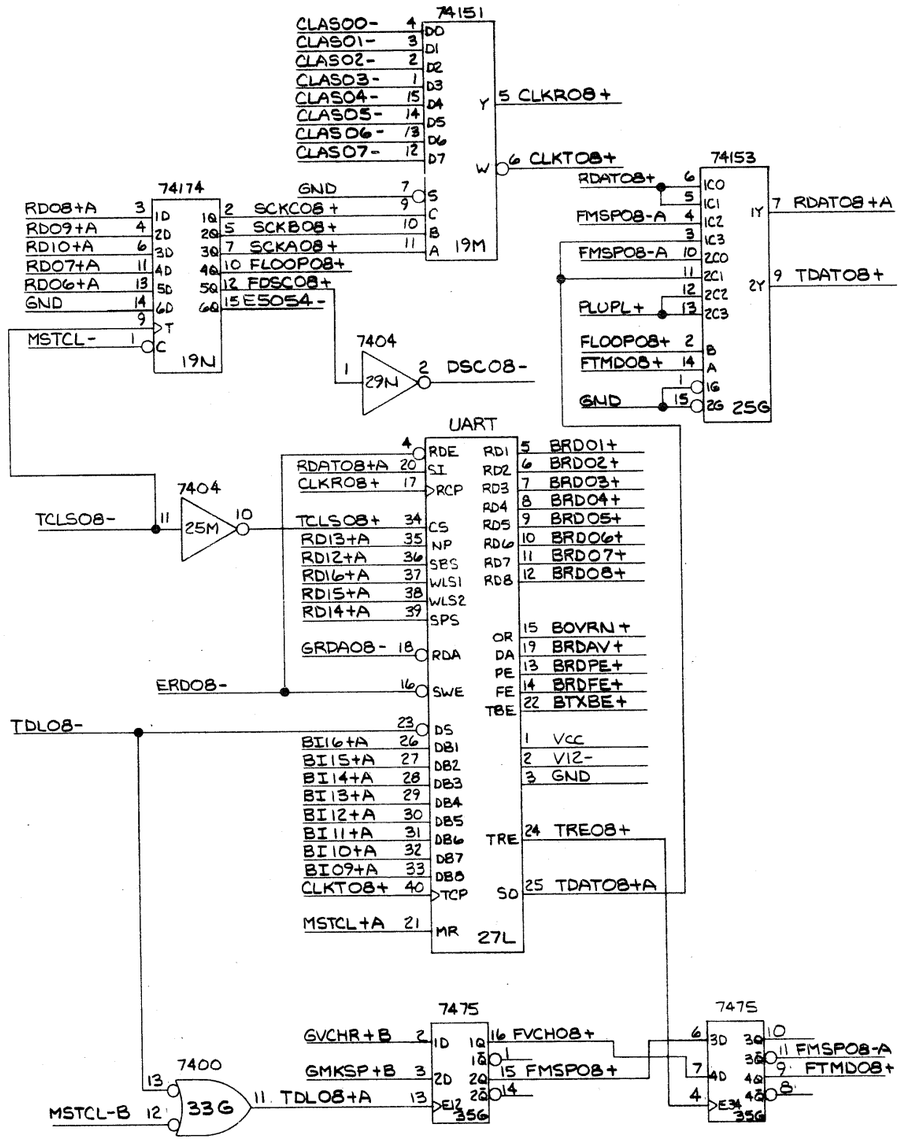
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

AMLC LINE INTERFACE
& CLOCK SELECT
(LINES 06 & 07) E.V

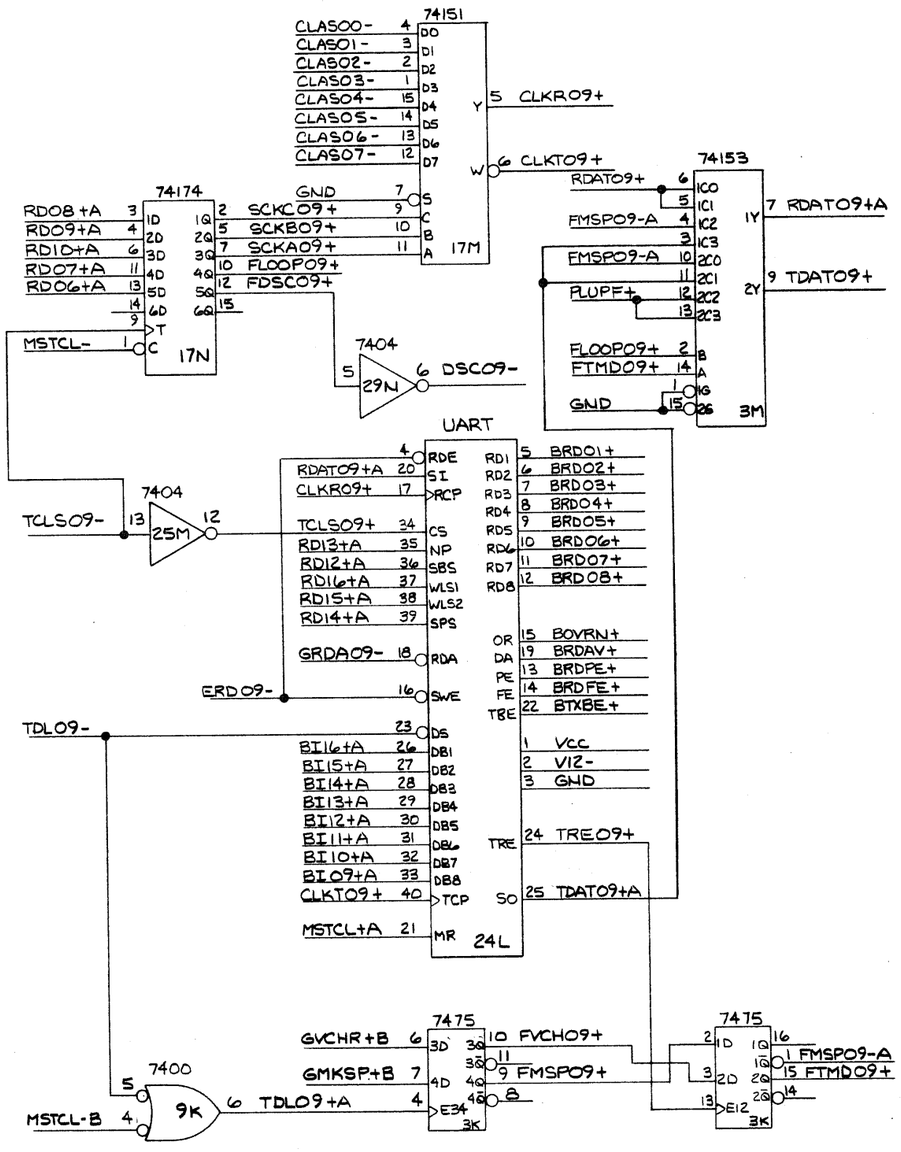
SHEET	SIZE	DWG. NO.	REV.
22 OF	C	LBD1735	D

PDF-003

LINE # 08



LINE # 09

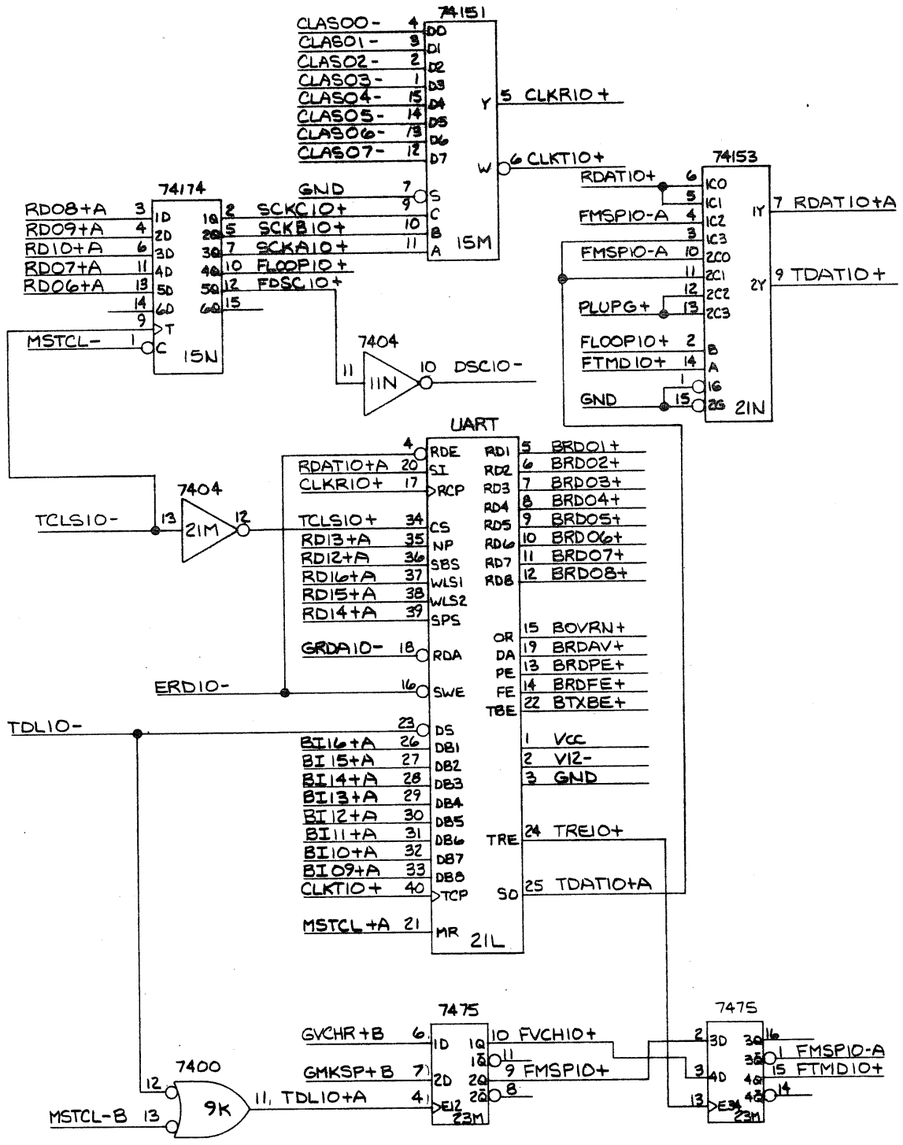


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

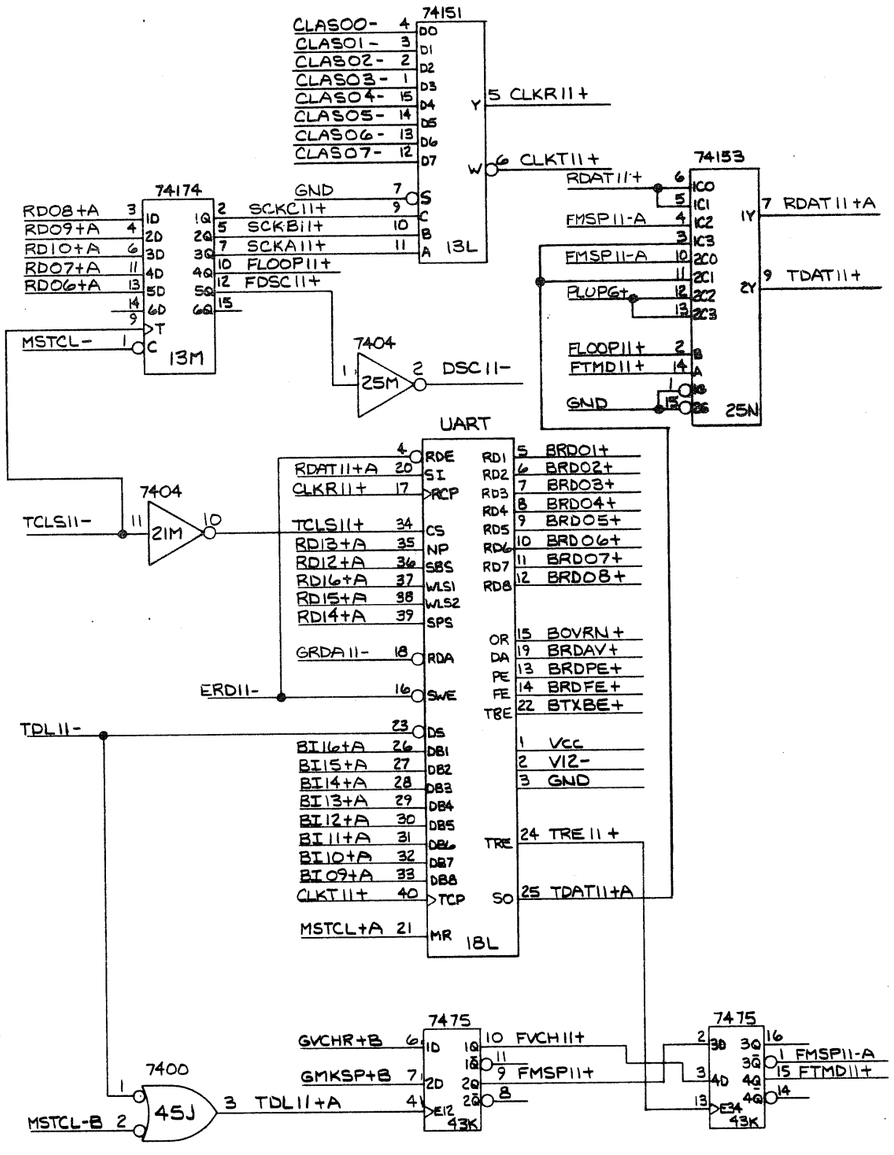
AMLC LINE INTERFACE
& CLOCK SELECT
(LINES 08 & 09) E.V

SHEET 23 OF | SIZE C | DWG. NO. LBD1735 | REV. C

LINE # 10



LINE # 11



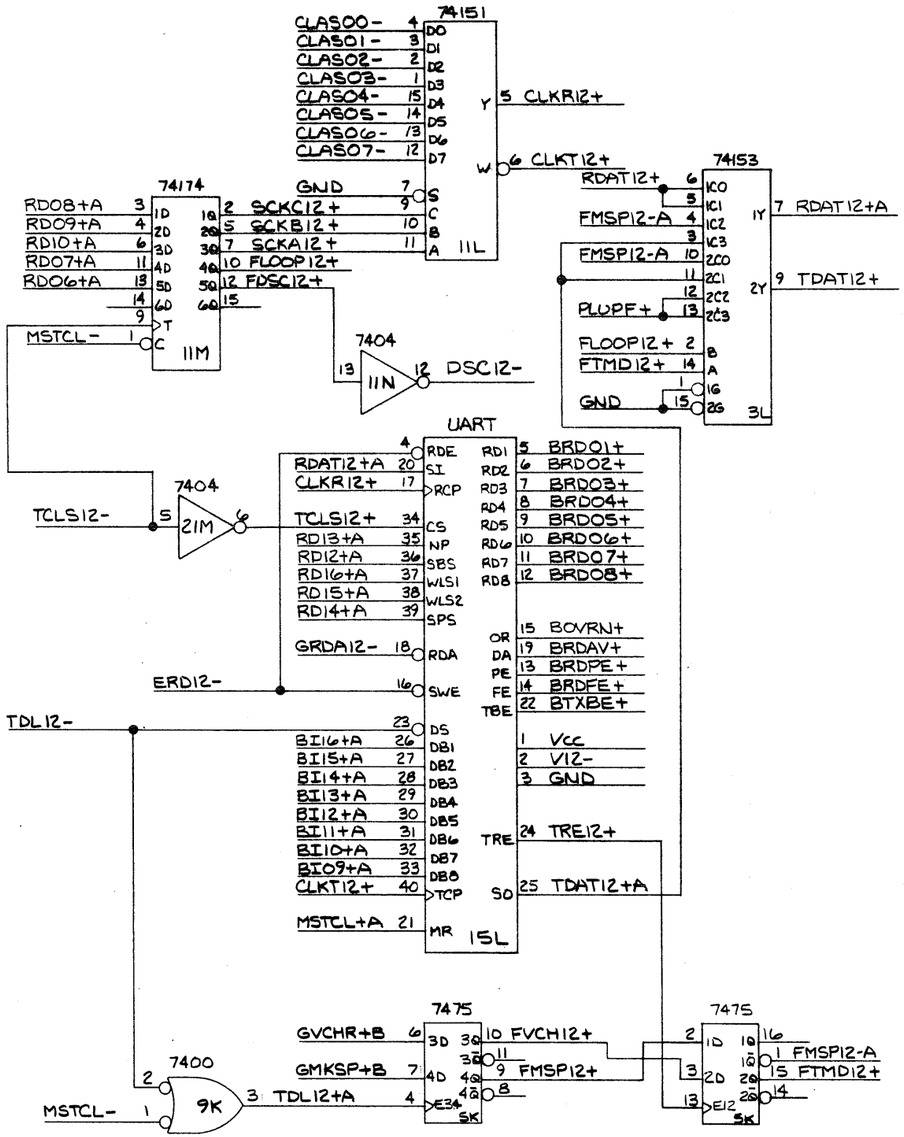
II-25

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

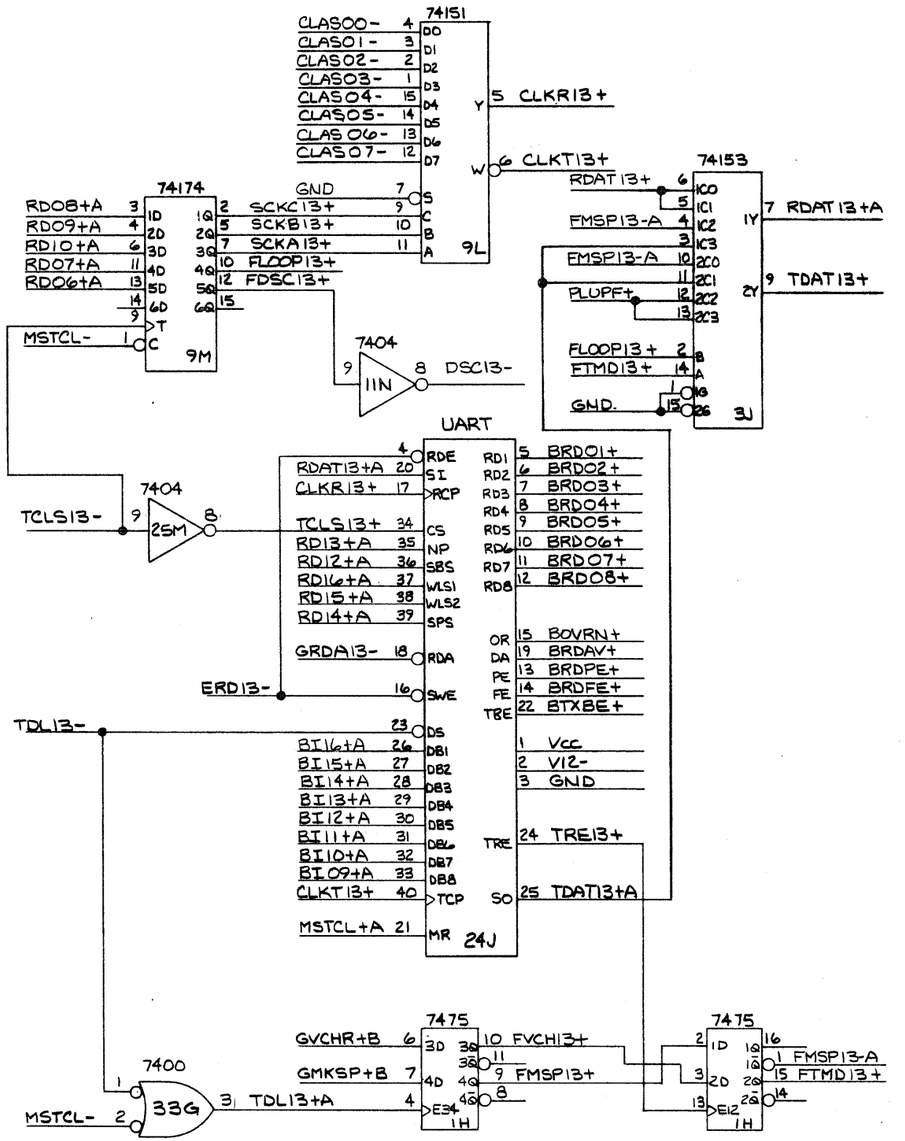
AMLC LINE INTERFACE
& CLOCK SELECT
(LINES 10 & 11) E.V

SHEET	OF	SIZE	DWG. NO.	REV.
24		C	LBD 1735	B

LINE # 12



LINE # 13



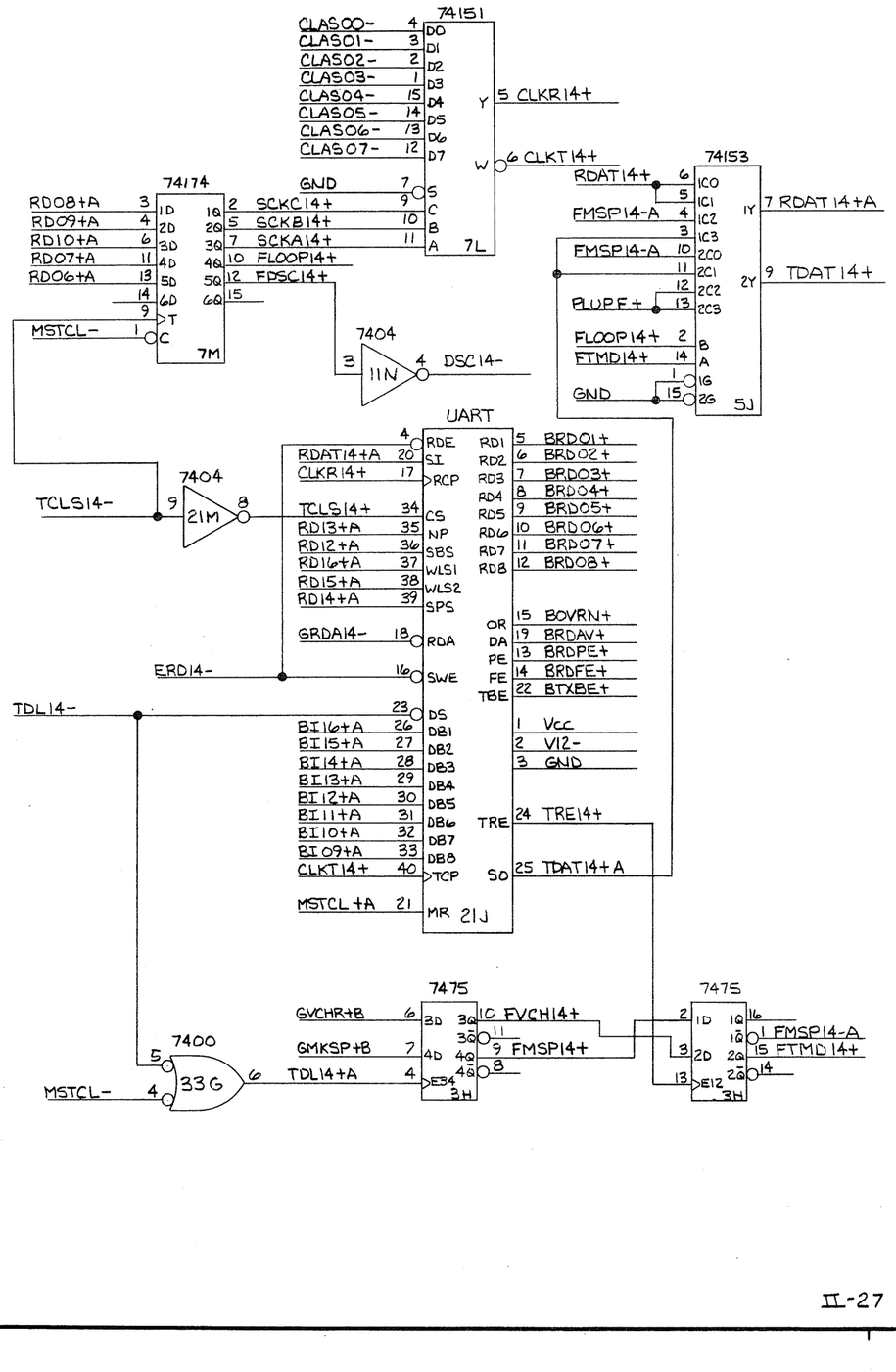
PDF-003

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

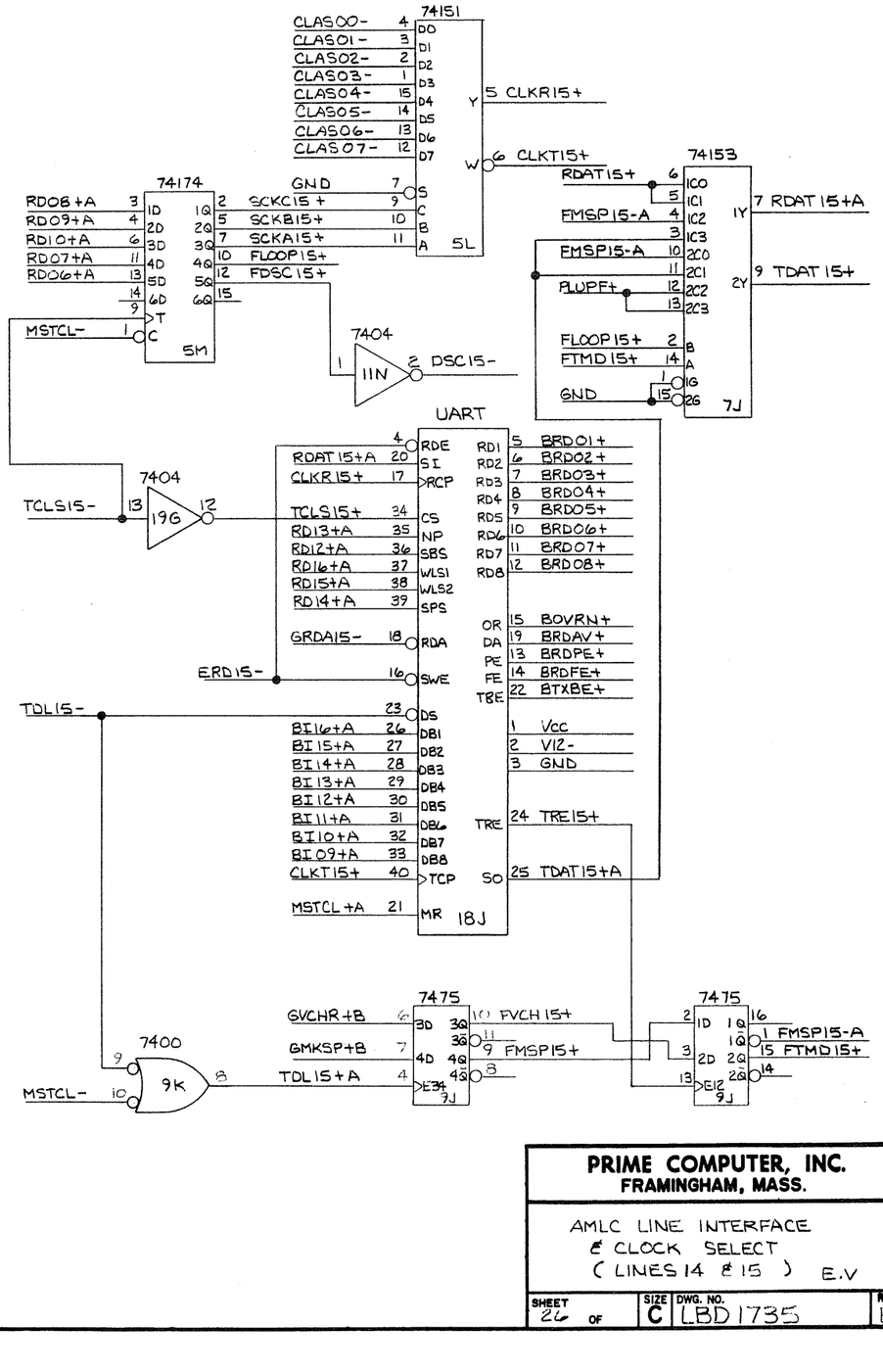
AMLC LINE INTERFACE
& CLOCK SELECT
(LINES 12 & 13) E.V

SHEET	SIZE	DWG. NO.	REV.
25 OF	C	LBD1735	B

LINE #14



LINE #15



PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

AMLC LINE INTERFACE
& CLOCK SELECT
(LINES 14 & 15) E.V

SHEET	OF	SIZE	DWG. NO.	REV.
26		C	LBD1735	B

PDF-003

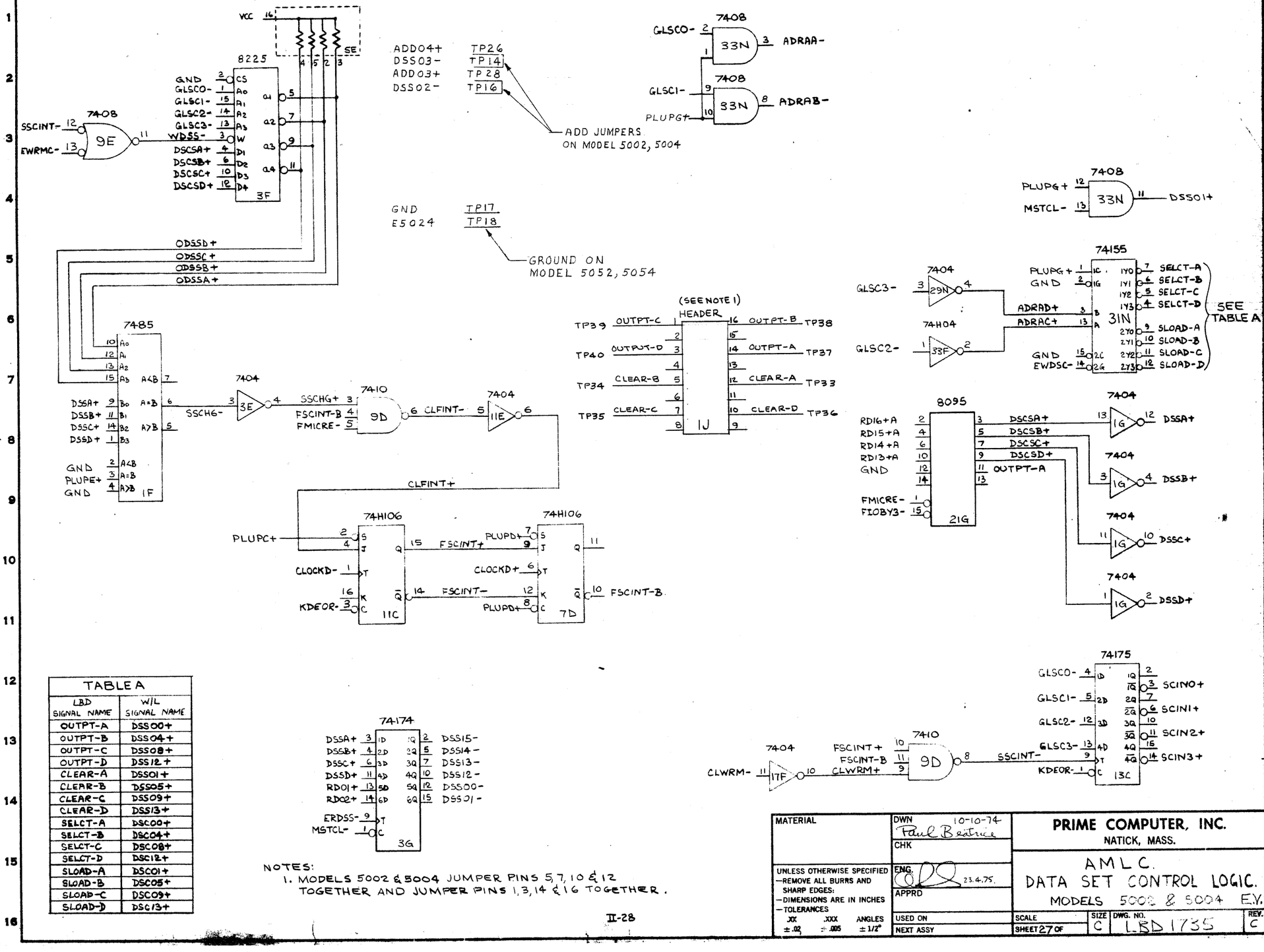
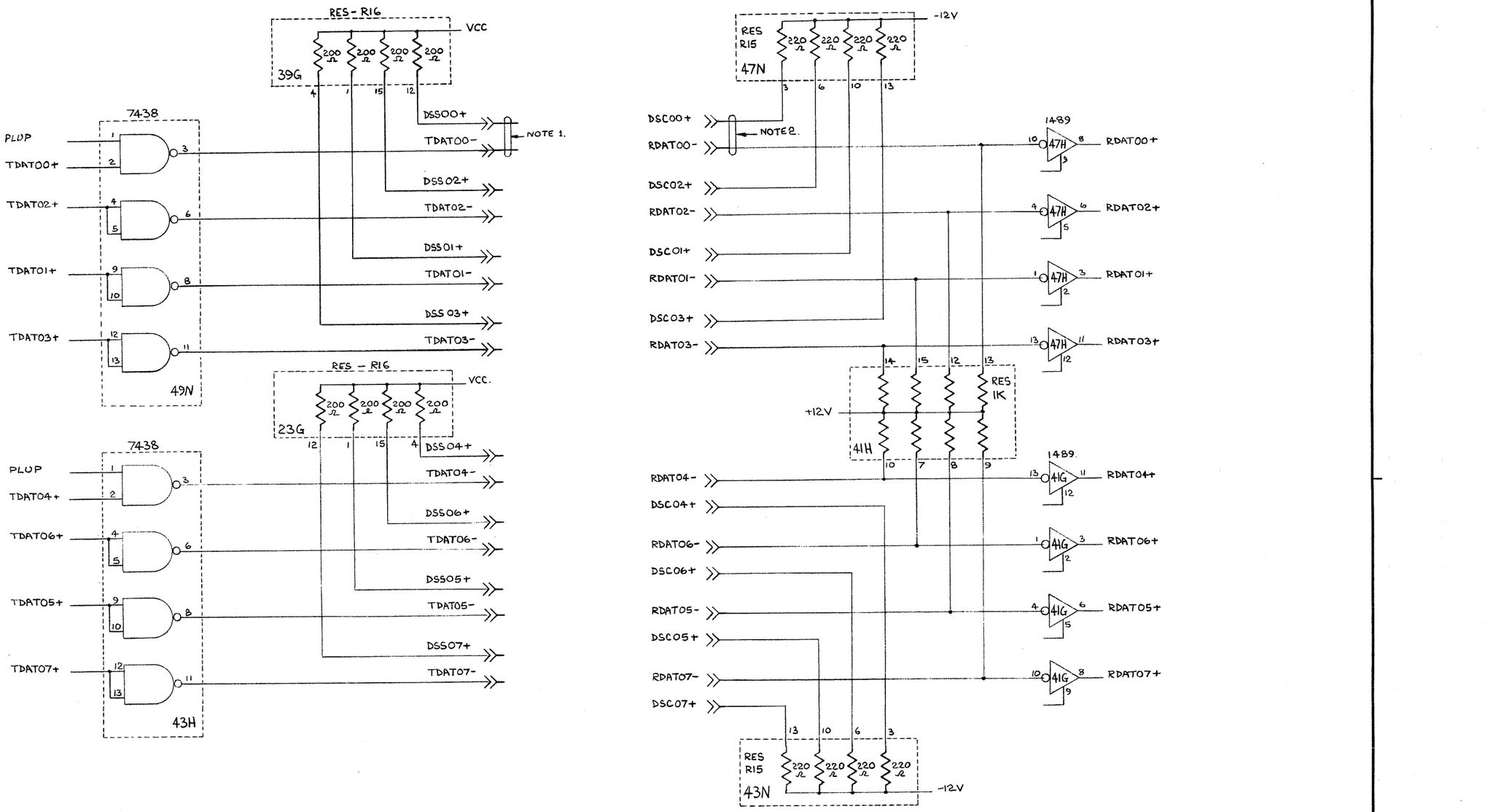


TABLE A	
LBD SIGNAL NAME	W/L SIGNAL NAME
OUTPT-A	DSS00+
OUTPT-B	DSS04+
OUTPT-C	DSS08+
OUTPT-D	DSS12+
CLEAR-A	DSS01+
CLEAR-B	DSS05+
CLEAR-C	DSS09+
CLEAR-D	DSS13+
SELCT-A	DSC00+
SELCT-B	DSC04+
SELCT-C	DSC08+
SELCT-D	DSC12+
SLOAD-A	DSC01+
SLOAD-B	DSC05+
SLOAD-C	DSC09+
SLOAD-D	DSC13+

NOTES:
1. MODELS 5002 & 5004 JUMPER PINS 5, 7, 10 & 12 TOGETHER AND JUMPER PINS 1, 3, 14 & 16 TOGETHER.

MATERIAL	DWN 10-10-74 Paul Beatrice	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG. 23.4.75.	AMLC. DATA SET CONTROL LOGIC. MODELS 5002 & 5004 E.V.	
	APPRD		
	USED ON	SCALE	SIZE C DWG. NO. LBD 1735 REV. C
	NEXT ASSY	SHEET 27 OF	

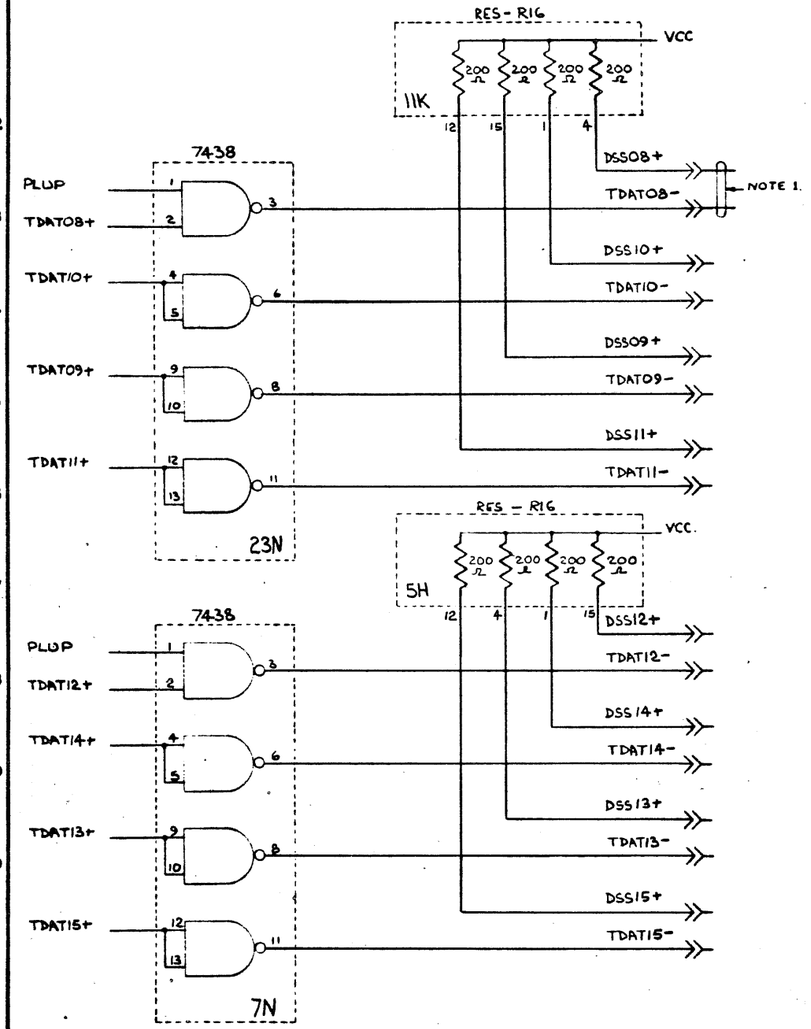
PDF-003

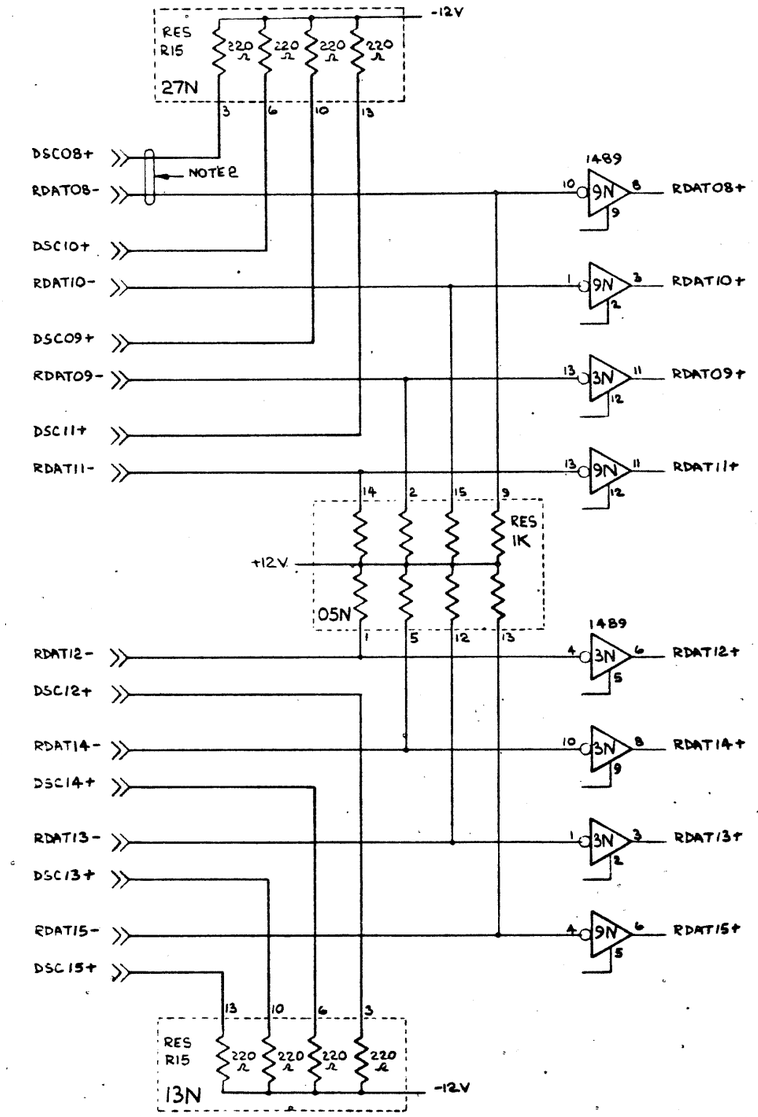


NOTES

1. EACH PAIR OF LEADS TDATXX-/DSSXX+ IS A 20MA CURRENT LOOP TRANSMIT PAIR.
2. EACH PAIR OF LEADS RDATXX-/DSCXX+ IS A 20MA CURRENT LOOP RECEIVE PAIR.

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	AMLC 20MA INTERFACE. LINES 0-7. MODELS 5074 & 5075	
	APPRD		
USED ON	SCALE	SIZE C	DWG. NO. LBD 1735 REV. B
NEXT ASSY	SHEET 28 OF		





NOTES

1. EACH PAIR OF LEADS TDATXX-/DSSXX+ IS A 20MA CURRENT LOOP TRANSMIT PAIR.
2. EACH PAIR OF LEADS RDATXX-/DSCXX+ IS A 20MA CURRENT LOOP RECEIVE PAIR.

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ± 1/2°	ENG 23.4.75.	AMLC 20MA INTERFACE. LINES 8-15. MODEL 5074
	APPRD	
USED ON / NEXT ASSY	SCALE / SHEET 29 OF	SIZE / DWG. NO. LBD 1735 / REV. B

LTR	DATE	REVISION	DR.	CK.

(SOLDER SIDE)

NAME		CONN PIN
VCC1		CA-1
VCC1		CA-2
SHIELD(GND)		CA-3
BPCPCPH+		CA-4
BPCPDEN+		CA-5
GND		CA-6
BPCPPND-		CA-7
BPCPPNA-		CA-8
BPCPPNB-		CA-9
BPCPPNC-		CA-10
BPCPPND-		CA-11
BPCPPNE-		CA-12
BPCPPNF-		CA-13
BPCPPNG-		CA-14
BPCPPNH-		CA-15
BPCIRN+		CA-16
BPCIPND-		CA-17
BPCIPNA-		CA-18
BPCIPNB-		CA-19
BPCIPNC-		CA-20
BPCIPND-		CA-21
SHIELD(GND)		CA-22
BPCICPN+		CA-23
GND		CA-24
BPCCRE+		CA-25
SHIELD(GND)		CA-26
		CA-27
		CA-28
		CA-29
BPCIOR+		CA-30
		CA-31
		CA-32
		CA-33
		CA-34
		CA-35
		CA-36
		CA-37
BPCIOW1-		CA-38
		CA-39
		CA-40
		CA-41
GND		CA-42
BMCWDLL+		CA-43
		CA-44
		CA-45
		CA-46
BMCWDLL+		CA-47
SHIELD(GND)		CA-48
VCC1		CA-49
VCC1		CA-50

NAME		CONN PIN
BMCADL+		CA-51
		CA-52
		CA-53
		CA-54
		CA-55
BMAPEL+		CA-56
BMAPER+		CA-57
BMDPEL-		CA-58
BMDPER-		CA-59
GND		CA-60
BMDO1+		CA-61
BMDO2+		CA-62
BMDO3+		CA-63
BMDO4+		CA-64
BMDO5+		CA-65
BMDO6+		CA-66
BMDO7+		CA-67
BMDO8+		CA-68
BMDO9+		CA-69
BMDI0+		CA-70
BMDI1+		CA-71
BMDI2+		CA-72
BMDI3+		CA-73
BMDI4+		CA-74
BMDI5+		CA-75
BMDI6+		CA-76
BMDLP-		CA-77
BMDRP-		CA-78
BMCSELB-		CA-79
BMCSELV-		CA-80
BMCWRB-		CA-81
BMCWRB-		CA-82
BMCRFSH-		CA-83
BMCEXS1-		CA-84
BMCWSTRB-		CA-85
BMCEXS2-		CA-86
BPCFCLK+		CA-87
BMCS3S1-		CA-88
BPCIRQ-		CA-89
BMCS3S2-		CA-90
BPCDRQ-		CA-91
BMCS3S3-		CA-92
BMCPRCH-		CA-93
BMCCNBL-		CA-94
GND		CA-95
VCC2		CA-96
VCC2		CA-97
GND		CA-98
VCC2		CA-99
VCC2		CA-100

NAME		CONN PIN
VCC1		CB-1
VCC1		CB-2
GND		CB-3
ISOLATED		CB-4
BMA99-		CB-5
BMA00-		CB-6
BMA01-		CB-7
BMA02-		CB-8
BMA04-		CB-9
BMA04-		CB-10
BMA05-		CB-11
BMA06-		CB-12
BMA07-		CB-13
BMA08-		CB-14
BMA09-		CB-15
BMA10-		CB-16
BMA11-		CB-17
BMA12-		CB-18
BMA13-		CB-19
BMA14-		CB-20
BMA15-		CB-21
BMA16-		CB-22
BMALP-		CB-23
BMARP-		CB-24
HPWRFL-		CB-25
GND		CB-26
VCORE1		CB-27
VCORE1		CB-28
BPA01+		CB-29
GND		CB-30
BPA02+		CB-31
BPA03+		CB-32
BPA04+		CB-33
BPA05+		CB-34
BPA06+		CB-35
BPA07+		CB-36
BPA08+		CB-37
BPA09+		CB-38
BPA10+		CB-39
BPA11+		CB-40
MSYSCLR-		CB-41
GND		CB-42
VCORE2		CB-43
VCORE2		CB-44
BPDPEL-		CB-45
GND		CB-46
BPDPER-		CB-47
BPAPEL-		CB-48
BPA99+		CB-49
BPA00+		CB-50

NAME		CONN PIN
BPAI2+		CB-51
BPAI3+		CB-52
BPAI4+		CB-53
BPAI5+		CB-54
BPAI6+		CB-55
BPAIP+		CB-56
GND		CB-57
BPARP+		CB-58
BPCPIO+		CB-59
BPAPER-		CB-60
BPC60CY+		CB-61
BPCREDY-		CB-62
BPDLP+		CB-63
		CB-64
BPDO1+		CB-65
BPDRP+		CB-66
BPDO2+		CB-67
BPDO3+		CB-68
BPDO4+		CB-69
BPDO5+		CB-70
BPDO6+		CB-71
BPDO7+		CB-72
BPDO8+		CB-73
BPDO9+		CB-74
BPDI0+		CB-75
BPDI1+		CB-76
VI2-		CB-77
VI2-		CB-78
BPDI2+		CB-79
GND		CB-80
BPDI3+		CB-81
BPDI4+		CB-82
BPDI5+		CB-83
BPDI6+		CB-84
BPCMOD0+		CB-85
BPCMOD1+		CB-86
BPCMOD2+		CB-87
BPCMOD3+		CB-88
BPCIMMD+		CB-89
BPCSCLK+		CB-90
VI2+		CB-91
VI2+		CB-92
HRUN-		CB-93
HRUN-		CB-94
BPC3TRB+		CB-95
GND		CB-96
VSS		CB-97
VSS		CB-98
VBB		CB-99
VBB		CB-100

(SOLDER SIDE)

NAME		CONN PIN
DSC03+		CC-1
GD37N		CC-2
DSCSA+		CC-3
GD18N		CC-4
DSC02+		CC-5
GD37N		CC-6
DSC01+		CC-7
GD37N		CC-8
DSC00+		CC-9
GD37N		CC-10
TDAT02-		CC-11
GD45D		CC-12
TDAT03-		CC-13
GD45P		CC-14
TDAT00-		CC-15
GD45P		CC-16
TDAT01-		CC-17
GD45P		CC-18
DSCSB+		CC-19
GD18N		CC-20
DSCSC+		CC-21
GD18N		CC-22
DSS03+		CC-23
GD41P		CC-24
DSS02+		CC-25
GD41P		CC-26
DSS01+		CC-27
GD41P		CC-28
DSS00+		CC-29
GD41P		CC-30
DSCSD+		CC-31
GD18N		CC-32
RDAT00-		CC-33
GD43P		CC-34
RDAT01-		CC-35
GD43P		CC-36
ADRAA-		CC-37
GD45L		CC-38
RDAT02-		CC-39
GD43P		CC-40
RDAT03-		CC-41
GD43P		CC-42
ADRAB-		CC-43
GD45L		CC-44

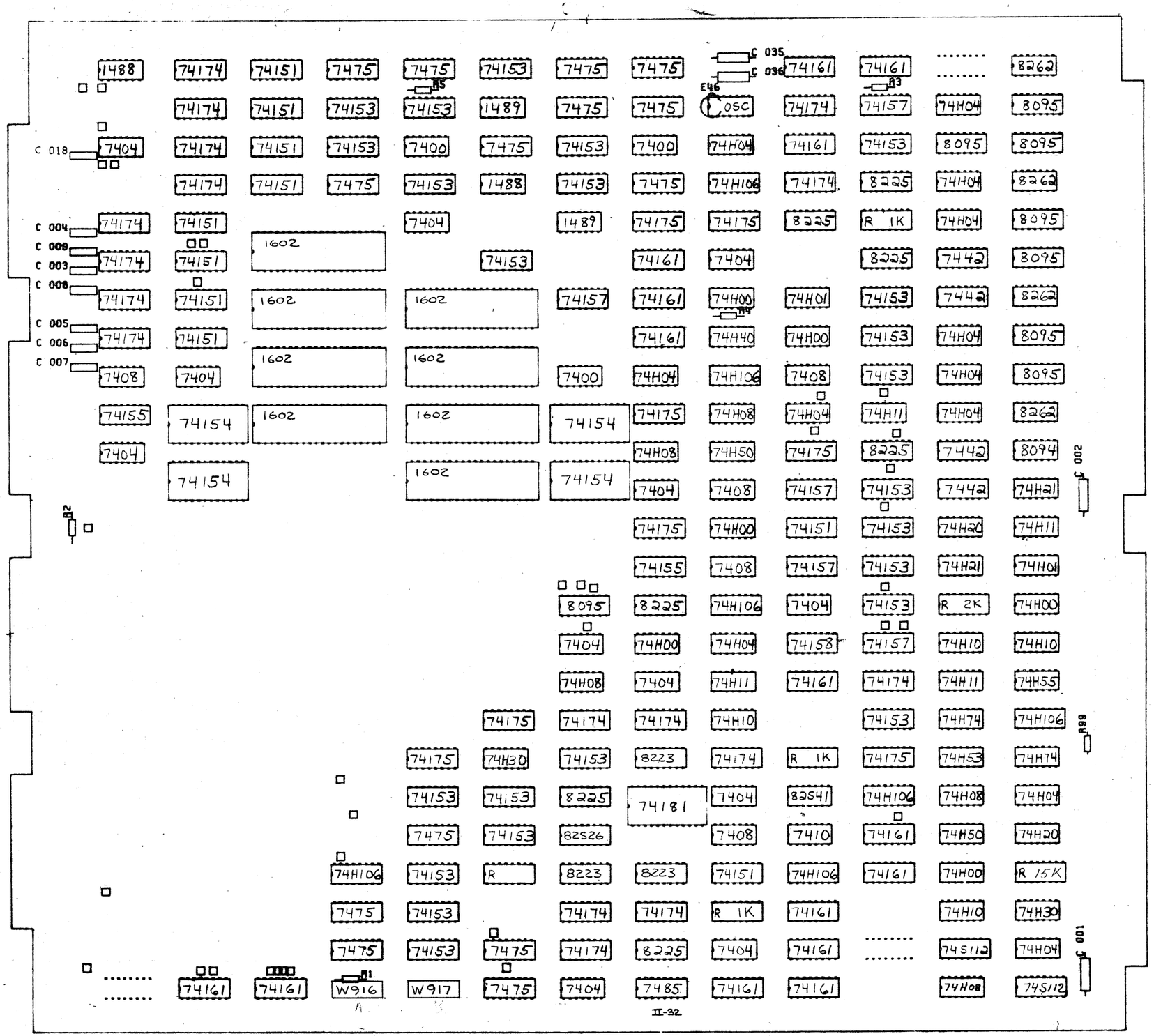
NAME		CONN PIN
DSC07+		CD-1
GD27P		CD-2
DSCSA+		CD-3
GD18N		CD-4
DSC06+		CD-5
GD27P		CD-6
DSC05+		CD-7
GD27P		CD-8
DSC04+		CD-9
GD27P		CD-10
TDAT06-		CD-11
GD35P		CD-12
TDAT07-		CD-13
GD35P		CD-14
TDAT04-		CD-15
GD35P		CD-16
TDAT05-		CD-17
GD35P		CD-18
DSCSB+		CD-19
GD18N		CD-20
DSCSC+		CD-21
GD18N		CD-22
DSS07+		CD-23
GD29P		CD-24
DSS06+		CD-25
GD29P		CD-26
DSS05+		CD-27
GD29P		CD-28
DSS04+		CD-29
GD29P		CD-30
DSCSD+		CD-31
GD18N		CD-32
RDAT04-		CD-33
GD31P		CD-34
RDAT05-		CD-35
GD31P		CD-36
ADRAA-		CD-37
GD45L		CD-38
RDAT06-		CD-39
GD31P		CD-40
RDAT07-		CD-41
GD31P		CD-42
ADRAB-		CD-43
GD45L		CD-44

NAME		CONN PIN
DSC11+		CE-1
GD16N		CE-2
DSCSA+		CE-3
GD18N		CE-4
DSC10+		CE-5
GD16N		CE-6
DSC09+		CE-7
GD16N		CE-8
DSC08+		CE-9
GD16N		CE-10
TDAT10+		CE-11
GD20P		CE-12
TDAT11-		CE-13
GD20P		CE-14
TDAT08-		CE-15
GD20P		CE-16
TDAT09-		CE-17
GD20P		CE-18
DSCSB+		CE-19
GD18N		CE-20
DSCSC+		CE-21
GD18N		CE-22
DSS11+		CE-23
GD16P		CE-24
DSS10+		CE-25
GD16P		CE-26
DSS09+		CE-27
GD16P		CE-28
DSS08+		CE-29
GD16P		CE-30
DSCSD+		CE-31
GD18N		CE-32
RDAT08-		CE-33
GD18P		CE-34
RDAT09-		CE-35
GD18P		CE-36
ADRAA-		CE-37
GD45L		CE-38
RDAT10-		CE-39
GD18P		CE-40
RDAT11-		CE-41
GD18P		CE-42
ADRAB-		CE-43
GD45L		CE-44

NAME		CONN PIN
DSC15+		CF-1
GD02L		CF-2
DSCSA+		CF-3
GD18N		CF-4
DSC14+		CF-5
GD02L		CF-6
DSC13+		CF-7
GD02L		CF-8
DSC12+		CF-9
GD02L		CF-10
TDAT14-		CF-11
GD10P		CF-12
TDAT15-		CF-13
GD10P		CF-14
TDAT12-		CF-15
GD10P		CF-16
TDAT13-		CF-17
GD10P		CF-18
DSCSB+		CF-19
GD18N		CF-20
DSCSC+		CF-21
GD18N		CF-22
DSS15+		CF-23
GD06P		CF-24
DSS14+		CF-25
GD06P		CF-26
DSS13+		CF-27
GD06P		CF-28
DSS12+		CF-29
GD06P		CF-30
DSCSD+		CF-31
GD18N		CF-32
RDAT12-		CF-33
GD08P		CF-34
RDAT13-		CF-35
GD08P		CF-36
ADRAA-		CF-37
GD45L		CF-38
RDAT14-		CF-39
GD08P		CF-40
RDAT15-		CF-41
GD08P		CF-42
ADRAB-		CF-43
GD45L		CF-44

DWG. NO. LBD1735 REV. A

MATERIAL	DWN 19 MAY 1977 J.F. TRAVALINI	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	CONNECTOR SIGNAL(E.V.) NAME LIST, AMLC
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE —— SIZE C DWG. NO. LBD1735 REV. A
		SHEET 30 OF



PRIME COMPUTER INC. NATICK, MASS.	AMLC MODEL Nº 5002 E.V.		
DWN Paul Benton 10-11-74		SIZE C	DWG. NO. LBD 1735
CHK		SCALE	REV. D
ENG.		SHEET 21 OF	
APPRD			
USED ON 5002-002			
NEXT ASSY 2076-001			

PRIME COMPUTER INC.
NATICK, MASS.

AMLC
MODEL 5004 EX.

DWN Paul Bastide 10-1-74
CHK
ENG
APPRD

USED ON 5004-002
NEXT ASSY 5018-002

SIZE C
DWG. NO. LBD1735
REV. D
SCALE
SHEET 32 OF

PRIME COMPUTER INC.	
NATICK, MASS.	
AMLC MODEL Nº 5052 E.V.	
DWN Paul B 10-11-74	
CHK	
ENG	
APPRD	
USED ON 5052-002	SIZE C DWG. NO. LBD1735 REV D
NEXT ASSY	SHEET 33 OF

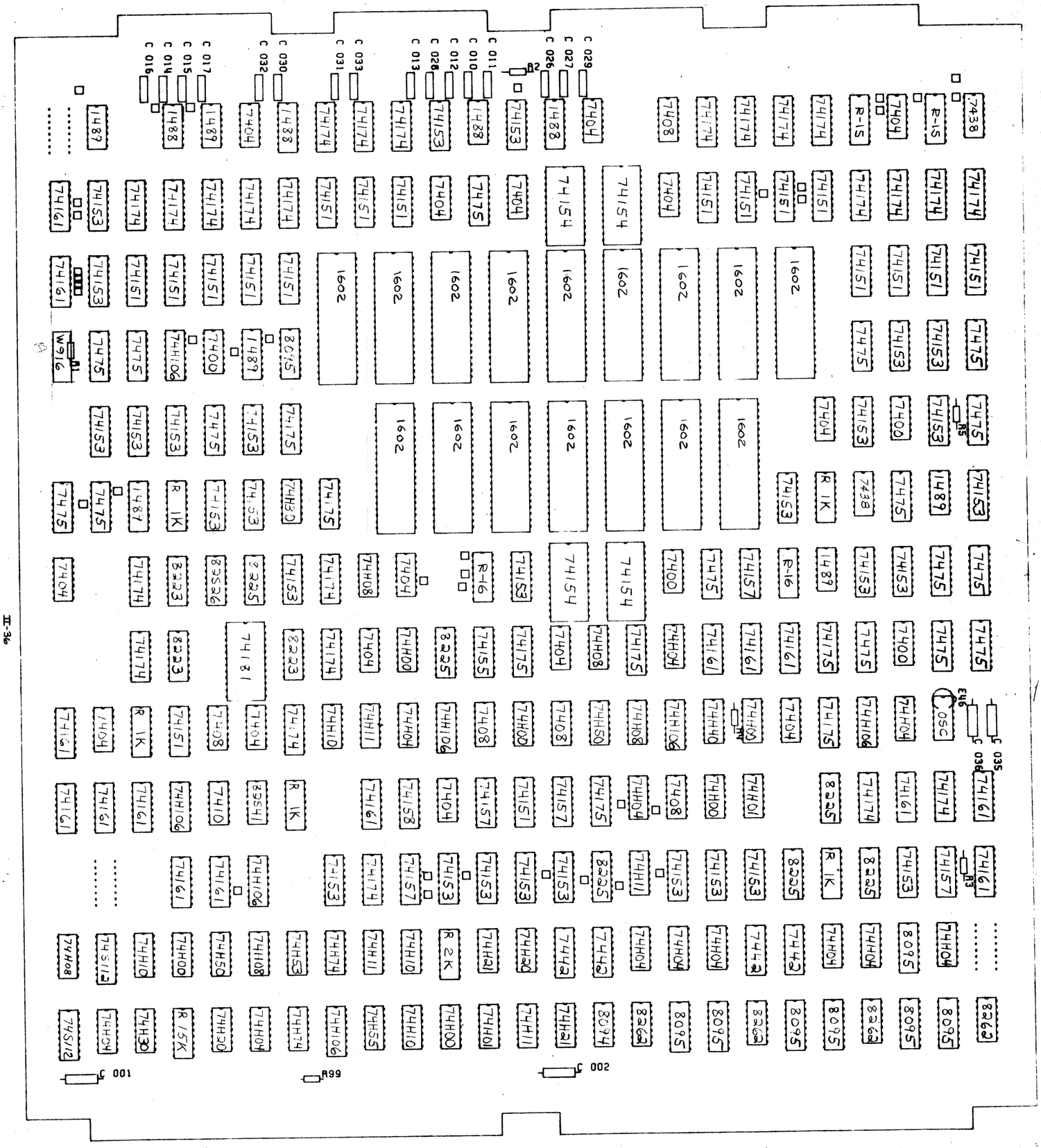
PRIME COMPUTER INC.
NATICK, MASS.

AMLC
MODEL Nº 5054

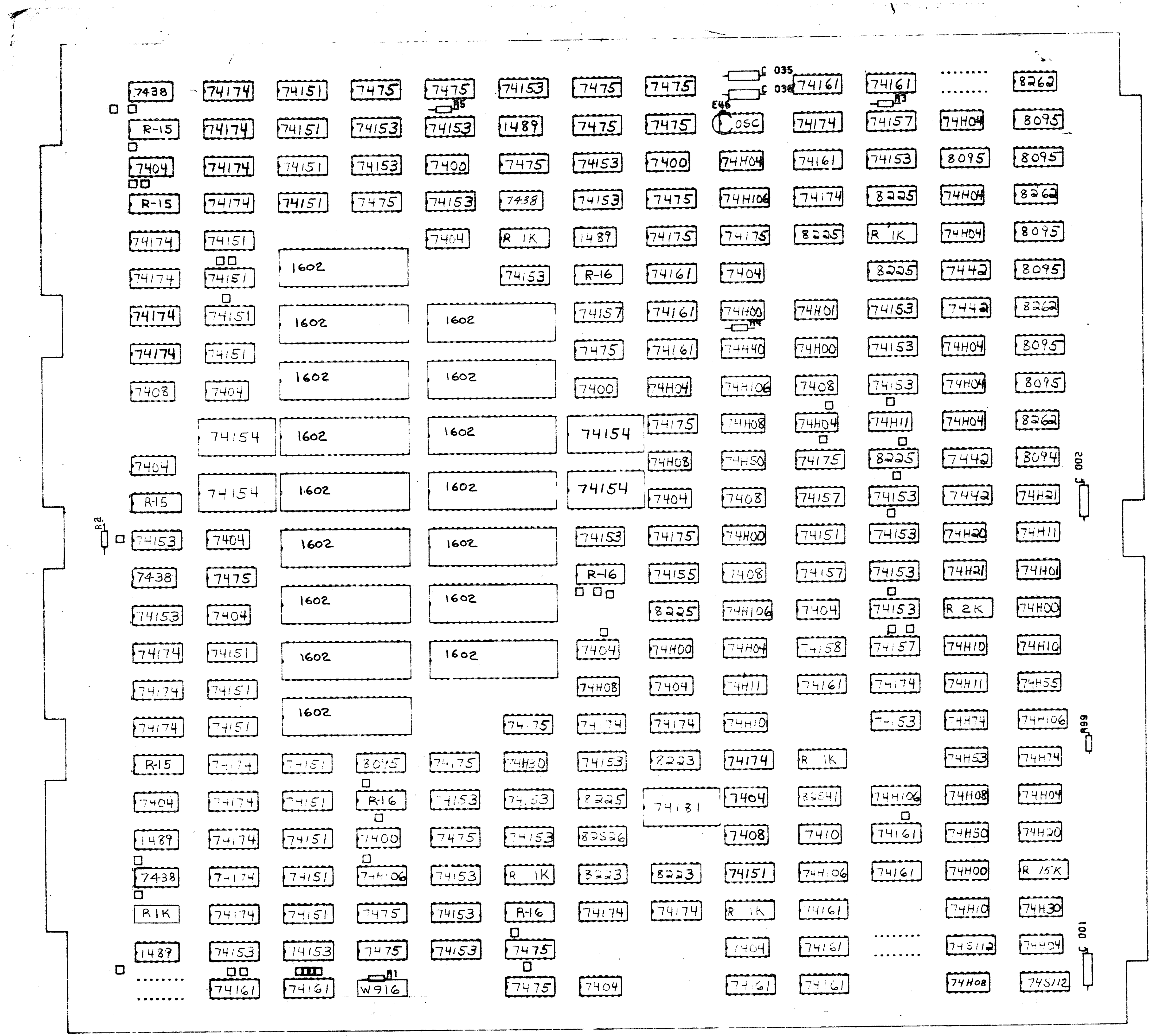
DWN 10-11-74
CHK
ENG
APPRD

USED ON 5054-CC2
NEXT ASSY

SIZE C
DWG. NO. LBD1735
SCALE
SHEET 34 OF
REV. C



DWN			PRIME COMPUTER INC.	
CHK			NATICK, MASS.	
APPRD			AMLC	
			MODEL Nº 5075	
USED ON	SCALE	SIZE	DWG. NO.	REV.
NEXT ASSY 5075-002	SHEET 35 OF	C	LBD 1735	E



PRIME COMPUTER INC.
NATICK, MASS.

AMLC
MODEL No 5074

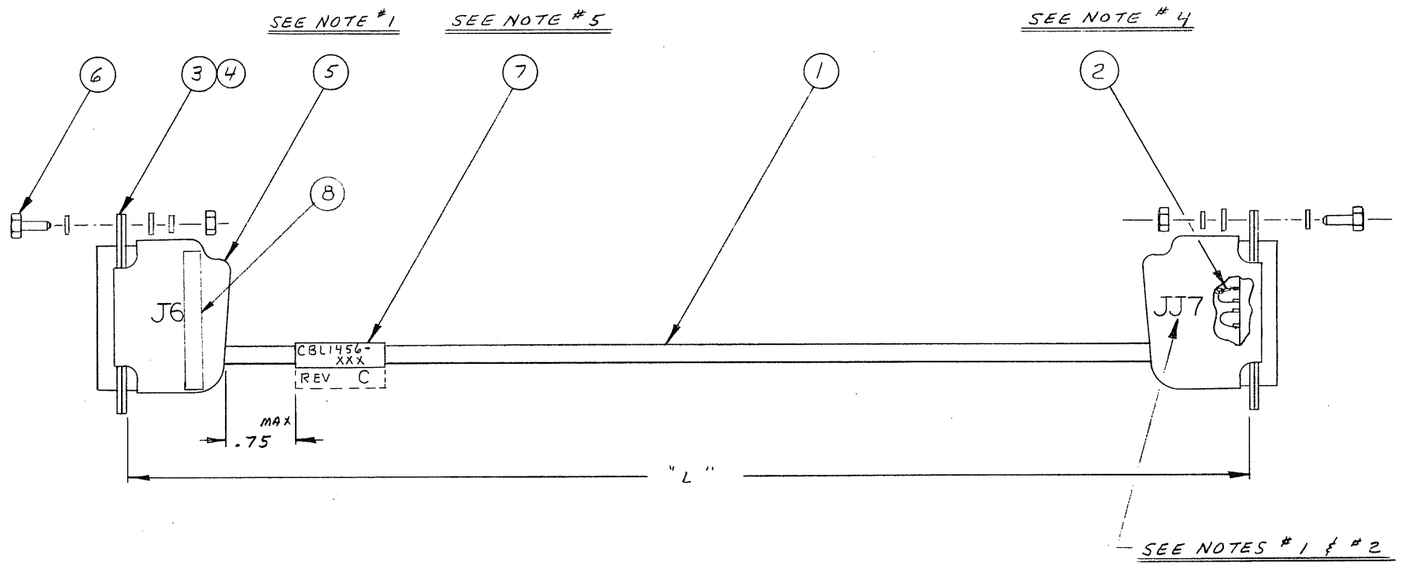
DWN	CHK	ENG	APPR'D	USED ON	NEXT ASSY	SCALE	SHEET 36 OF	SIZE C	DWG. NO. LBD 1735	REV. E

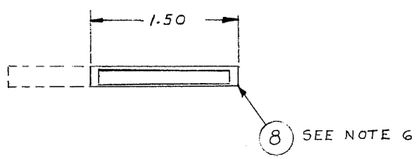
PRIME COMPUTER INC.	
NATICK, MASS.	
AMLC	
MODEL Nº 5072	
SIZE C	DWG. NO. LBD1735
SCALE	REV. C
SHEET 37 OF	
USED ON	
NEXT ASSY 5107	
DWN	12/1/75
CHK	
ENG	1.16.76
APPRD	

WIRE LIST			
FROM	TO	COLOR	COMMENTS
J6-Ø2	JJ7-Ø3	BLACK	
J6-Ø3	JJ7-Ø2	WHITE	
J6-2Ø	JJ7-Ø9	BROWN	SEE NOTE 7 ⚠
J6-Ø8	JJ7-Ø8	RED	SEE NOTE #4 ⚠
J6-Ø7	JJ7-Ø7	GREEN	

JUMPER LIST			
FROM	TO	COLOR	COMMENTS
JJ7-Ø4	JJ7-Ø5	RED	
JJ7-Ø8	JJ7-2Ø	RED	SEE NOTE #4

LTR	DATE	REVISION	DR.	CK.
A	3/14/75	RELEASED	JCTm	JCTm
B	4/16/75	REVISED PER ECN 1566	WB	JCTm
C	9/2/75	PER ECN 1628	WB	JCTm





-940	40FT ± 2FT
-022	62FT ± 2FT
-021	52FT ± 2FT
-020	10FT ± 6IN
-001	6IN ± 2IN
-XXX	"L" (LENGTH)

NOTES:
1. STAMP MARKINGS J6 & JJ7 IN WHITE INK .19 HIGH POSITIONED APPROXIMATELY AS SHOWN.
2. JJ MARKINGS INDICATE JUMPER END OF CABLE.
3. EQUIVALENT CONNECTORS MAY BE SUBSTITUTED
4. PIGTAIL RED WIRE FROM ITEM #1 & JUMPER TO JJ7-08.
5. TYPE PART NO AND REV IN BLACK ON ITEM #7 AS SHOWN.
6. CUT ITEM 8 TO DIM SHOWN, TYPE IN BLACK IN SPACE PROVIDED THE WORD "CONTROLLER", LOCATE ON J6 APPROX AS SHOWN.
⚠7. WHEN ALPHA WIRE IS USED THE BROWN WIRE IS ORANGE.

MATERIAL: SEE BOM

UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES:
—DIMENSIONS ARE IN INCHES
—TOLERANCES
.XX ±.02 .XXX ±.005 ANGLES ±1/2°

DWN JCTm 5/6/74
CHK
ENG. 3.14.75
APPRD
USED ON
NEXT ASSY

PRIME COMPUTER, INC.
NATICK, MASS.

CABLE, FEMALE EIA TO FEMALE EIA

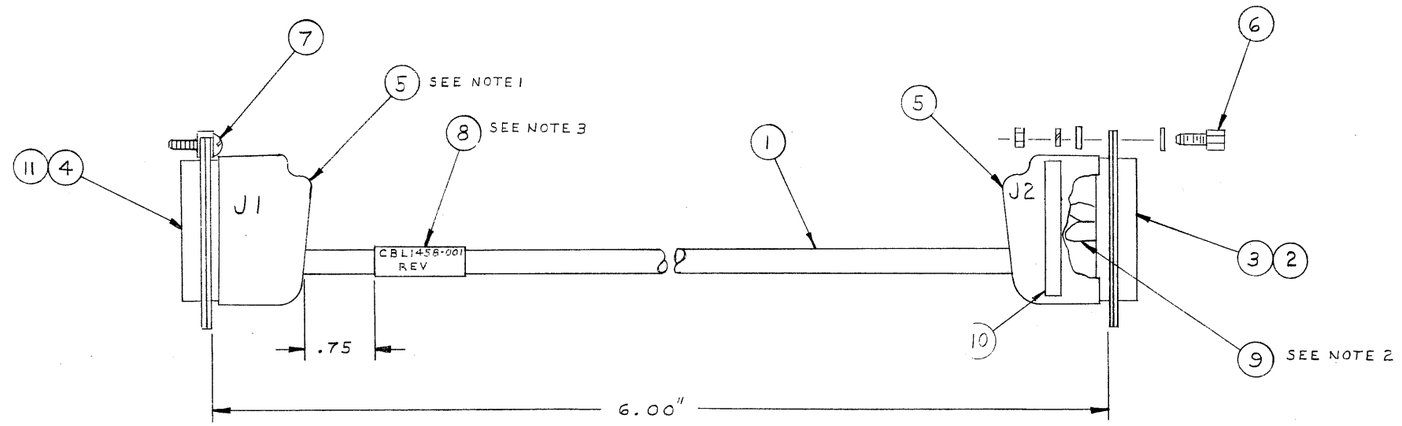
SCALE NONE SHEET 1 OF 1 SIZE C DWG. NO. CBL1456-XXX REV. C

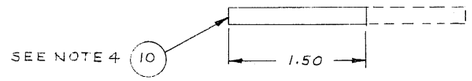
DWG. NO. CBL1456-XXX REV. C

III-1

WIRE LIST			
FROM	TO	COLOR	COMMENT
J1-2	J2-2	RED	
J1-3	J2-3	GRN	
J1-7	J2-7	BLK	
J1-8	J2-11	BRN	
J1-9	J2-9	WHT	
J2-6	J2-8*	RED	JUMPER
J2-8*	J2-20	RED	JUMPER

LTR	DATE	REVISION	DR.	CK.





NOTES:-

1. STAMP MARKINGS J1 & J2 .19 HIGH WITH WHITE INK. LOCATE APPROX AS SHOWN.
2. * DOUBLE CRIMP WIRES ON PIN 8 OF J2.
3. TYPE PART NO. AND REVISION IN BLACK ON ITEM 8 AS SHOWN.
4. CUT ITEM 10 TO DIM SHOWN, TYPE IN BLACK IN SPACE PROVIDED THE WORDS "L. PRINTER" LOCATE ON J2 APPROX AS SHOWN.

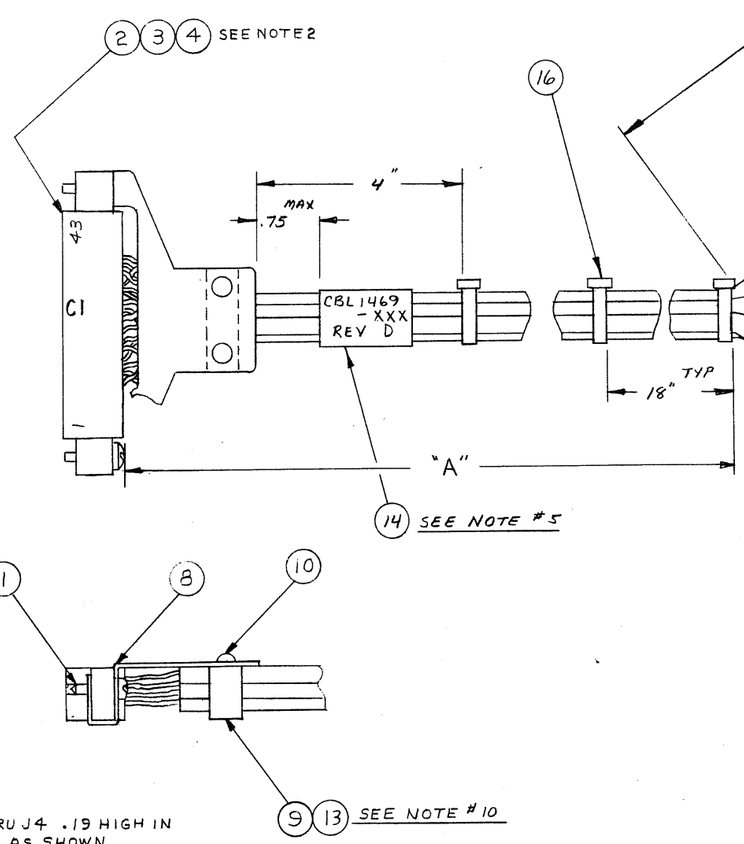
MATERIAL: SEE BOM	DWN W Bogan 5/13/75	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK 5/13/75	CABLE, ADAPTER FEMALE EIA TO CENTRONIC PRINTER
	ENG. 6.19.75	
	APPRD	
	USED ON NEXT ASSY 3127-902	SCALE NONE SHEET 1 OF 1 SIZE C DWG. NO. CBL1458-001 REV. A

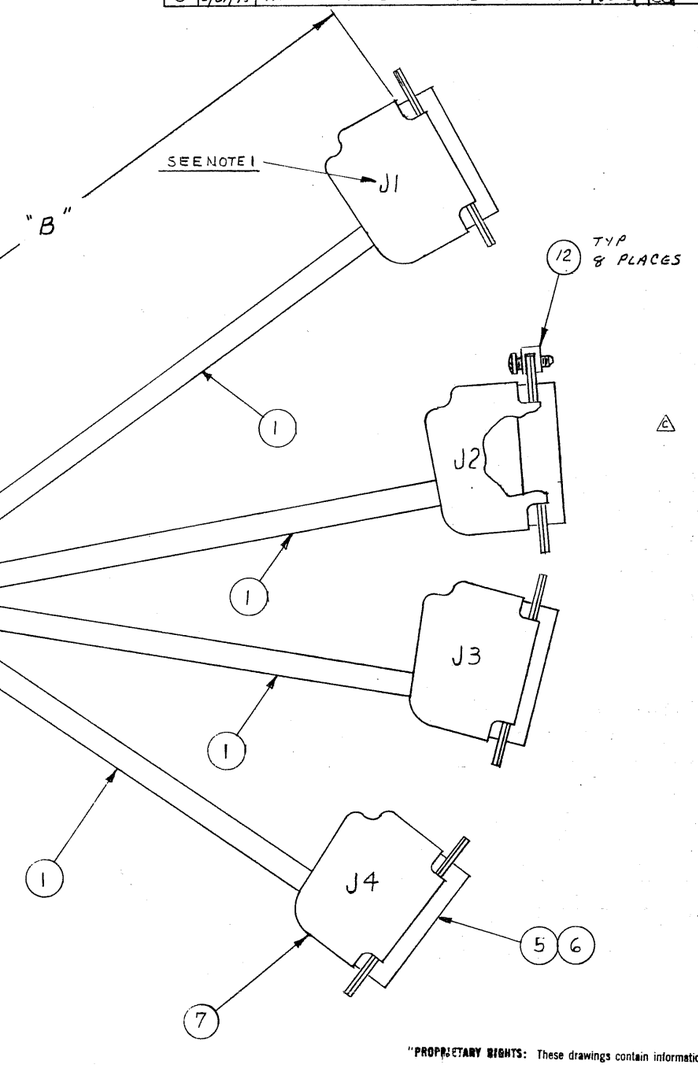
DWG. NO. CBL1458-001 REV. A

WIRE LIST			
FROM	TO	COLOR	COMMENTS
C1-15	J1-2	RED	
C1-16	J1-7	BLACK	
C1-33	J1-3	GREEN	
C1-9	J1-20	WHITE	△6
C1-29	J1-8	BROWN	NOTE 11 △4
			△5
C1-17	J2-2	RED	
C1-18	J2-7	BLACK	
C1-35	J2-3	GREEN	
C1-7	J2-20	WHITE	△6
C1-27	J2-8	BROWN	NOTE 11 △4
			△6
C1-11	J3-2	RED	
C1-12	J3-7	BLACK	
C1-39	J3-3	GREEN	
C1-5	J3-20	WHITE	△6
C1-25	J3-8	BROWN	NOTE 11 △4
			△6
C1-13	J4-2	RED	
C1-14	J4-7	BLACK	
C1-41	J4-3	GREEN	
C1-1	J4-20	WHITE	△6
C1-23	J4-8	BROWN	NOTE 11 △6 △4

LTR	DATE	REVISION	DR.	CK.
D	8/17/73	ECN 1628 & 1675	XB	JGL
D_2	6-11-74	-902 ADDED	JPK	JGL

LTR	DATE	REVISION	DR.	CK.
A	8/1/73	RELEASED	JGL	JGL
B	12/18/73	REDESIGNED & PART # FROM 5031 ECN 1259	JGL	JGL
C	2/27/75	WIRE LIST REVISED PER ECR 1487	JGL	QP





NOTES:
1. STAMP MARKINGS C1, J1 THRU J4 .19 HIGH IN WHITE INK. POSITION APPROX AS SHOWN.
2. INSERT KEY, ITEM 4 BETWEEN SLOTS 25/26 & 27/28 OF ITEM 2.
3. EQUIVALENT CONNECTORS MAY BE SUBSTITUTED.
△4.
5. TYPE PART # AND REVISION IN BLACK ON ITEM 14 AS SHOWN.
6.
7.
8. FOR SIGNAL NAMES REFER TO LBD 1208.
9. SEE DWG INS 1210 FOR CABLE CODING LOCATION.
10. INSTALL ITEM 13 IN CUTOUT OF ITEM 9 TO INSURE TIGHT FIT OF CABLE.
△11. WHEN ALPHA WIRE IS USED THE BROWN WIRE IS ORANGE.

△2 -902	9' ±6"	191' ± 4'
△1 -901	9' ±6"	66' ± 2'
-001	9' ±6"	21' ± 1'
-XXX	DIM. "A"	DIM. "B"

III-3

MATERIAL: SEE BOM

UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES:
—DIMENSIONS ARE IN INCHES
—TOLERANCES
.XX ±.02 .XXX ±.005 ANGLES ±1/2°

DWN Jr. Logan 8/2/73
CHK J.G. Lucas 2/27/75
ENG. 2-27-75
APPRD. 2/27/75
USED ON
NEXT ASSY

PRIME COMPUTER, INC.
NATICK, MASS.

CABLE AMLC TO DATA SET TYPE 103A 4 EIA CONNECTORS

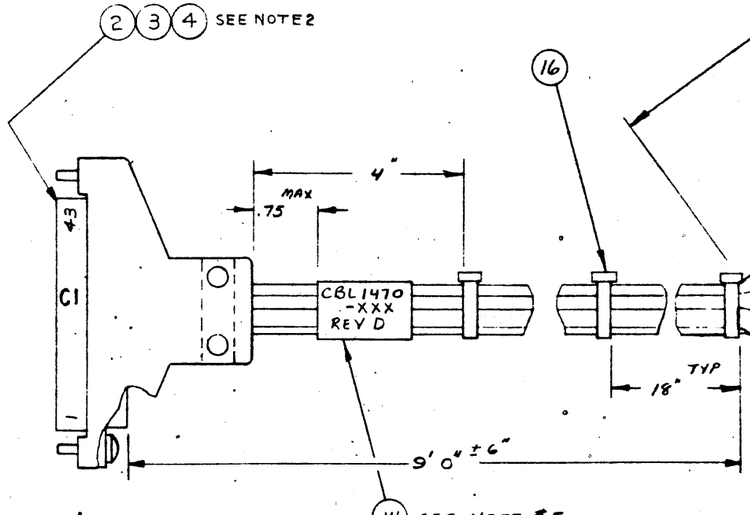
SCALE NONE SIZE C DWG. NO CBL1469-XXX REV. D_2
SHEET 1 OF 1

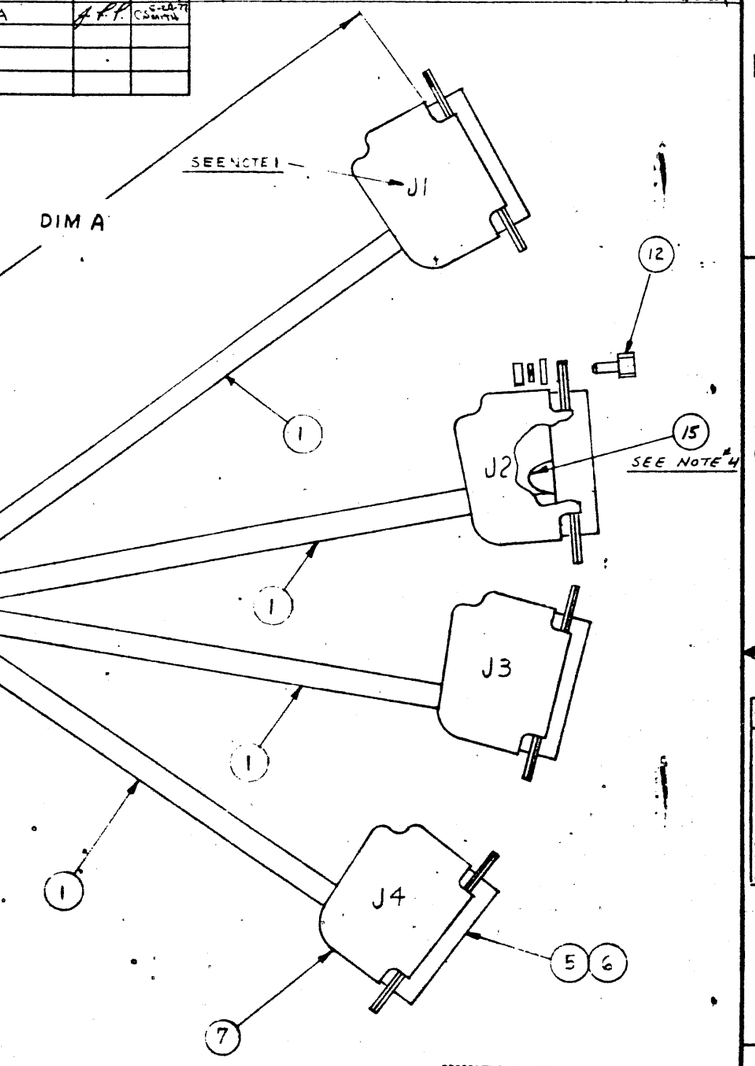
DWG. NO. CBL1469-001 REV. D_2

WIRE LIST			
FROM	TO	COLOR	COMMENTS
C1-15	J1-3	GRN	
C1-16	J1-7	BLACK	
C1-33	J1-2	RED	
C1-9	J1-9	WHITE	
C1-29	J1-8*	BROWN	SEE NOTE 11
J1-8*	J1-20	RED	JUMPER ⚠6
J1-4	J1-5	RED	JUMPER
J1-20*	J1-6	RED	JUMPER ⚠6
C1-17	J2-3	GRN	
C1-18	J2-7	BLACK	
C1-35	J2-2	RED	
C1-7	J2-9	WHITE	
C1-27	J2-8*	BROWN	SEE NOTE 11
J2-4	J2-5	RED	JUMPER
J2-8*	J2-20*	RED	JUMPER ⚠6
J2-20*	J2-6	RED	JUMPER ⚠6
C1-11	J3-3	GRN	
C1-12	J3-7	BLACK	
C1-39	J3-2	RED	
C1-5	J3-9	WHITE	
C1-25	J3-8*	BROWN	SEE NOTE 11
J3-4	J3-5	RED	JUMPER
J3-8*	J3-20*	RED	JUMPER ⚠6
J3-20*	J3-6	RED	JUMPER ⚠6
C1-13	J4-3	GRN	
C1-14	J4-7	BLACK	
C1-41	J4-2	RED	
C1-1	J4-9	WHITE	
C1-23	J4-8*	BROWN	SEE NOTE 11
J4-4	J4-5	RED	JUMPER
J4-8*	J4-20*	RED	JUMPER ⚠6
J4-20*	J4-6	RED	JUMPER ⚠6

LTR	DATE	REVISION	DR	CK
D	9/12/75	PER ECN 1628	KB	JCM
D1	5/4/76	ADDED -005 & -007	K.T.S.	JCM
D2	6/8/76	ADDED -950	K.T.S.	JCM
E	5-24-77	REVISED PER ECR 2241-A	K.P.	C-LA-77 COMMON

LTR	DATE	REVISION	DR.	CK.
A	9/4/73	RELEASED	JCM	JCM
B	11/18/73	REDRAWN PER ECN 1259	JCM	JCM
C	6/3/75	PER ECN 1606	KB	JCM





-950	141 FT ± 2FT	150 FT
-023	111 FT ± 2FT	120 FT
-022	101 FT ± 2FT	110 FT
-021	96 FT ± 2FT	105 FT
-020	93 FT ± 2FT	102 FT
-007	66 FT ± 2 FT	75 FT
-005	41 FT ± 1 FT	50 FT
-001	21 FT ± 1 FT	30 FT
-XXX	DIM A	TOTAL LENGTH REF

NOTES:
1. STAMP MARKINGS C1, J1 THRU J4 .19 HIGH IN WHITE INK. POSITION APPROX AS SHOWN.
2. INSERT KEY, ITEM 4 BETWEEN SLOTS 25/26 & 27/28 OF ITEM 2.
3. EQUIVALENT CONNECTORS MAY BE SUBSTITUTED.
* 4. DOUBLE CRIMP WIRES ON PIN 8 AND PIN 20 OF J1, J2, J3 & J4. USING ITEM 6
5. TYPE PART # AND REVISION IN BLACK ON ITEM 14 AS SHOWN.
6.
7.
8. FOR SIGNAL NAMES REFER TO LBD 1208.
9. SEE DWG ENS 1210 FOR CABLE CODING LOCATION.
10. INSTALL ITEM 13 IN CUTOUT OF ITEM 9 TO INSURE TIGHT FIT OF CABLE.
⚠ 11. WHEN ALPHA WIRE IS USED THE BROWN WIRE IS ORANGE.

III-4

MATERIAL	SEE BOM
DWN	K. Bowen 8/12/75
CHK	J.C. McGuire 6/24/75
ENG.	
APPRD	
USED ON	
NEXT ASSY	

UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES
—DIMENSIONS ARE IN INCHES
—TOLERANCES
.XX ±.02 .XXX ±.005 ANGLES ±1/2°

PRIME COMPUTER, INC.
NATICK, MASS.

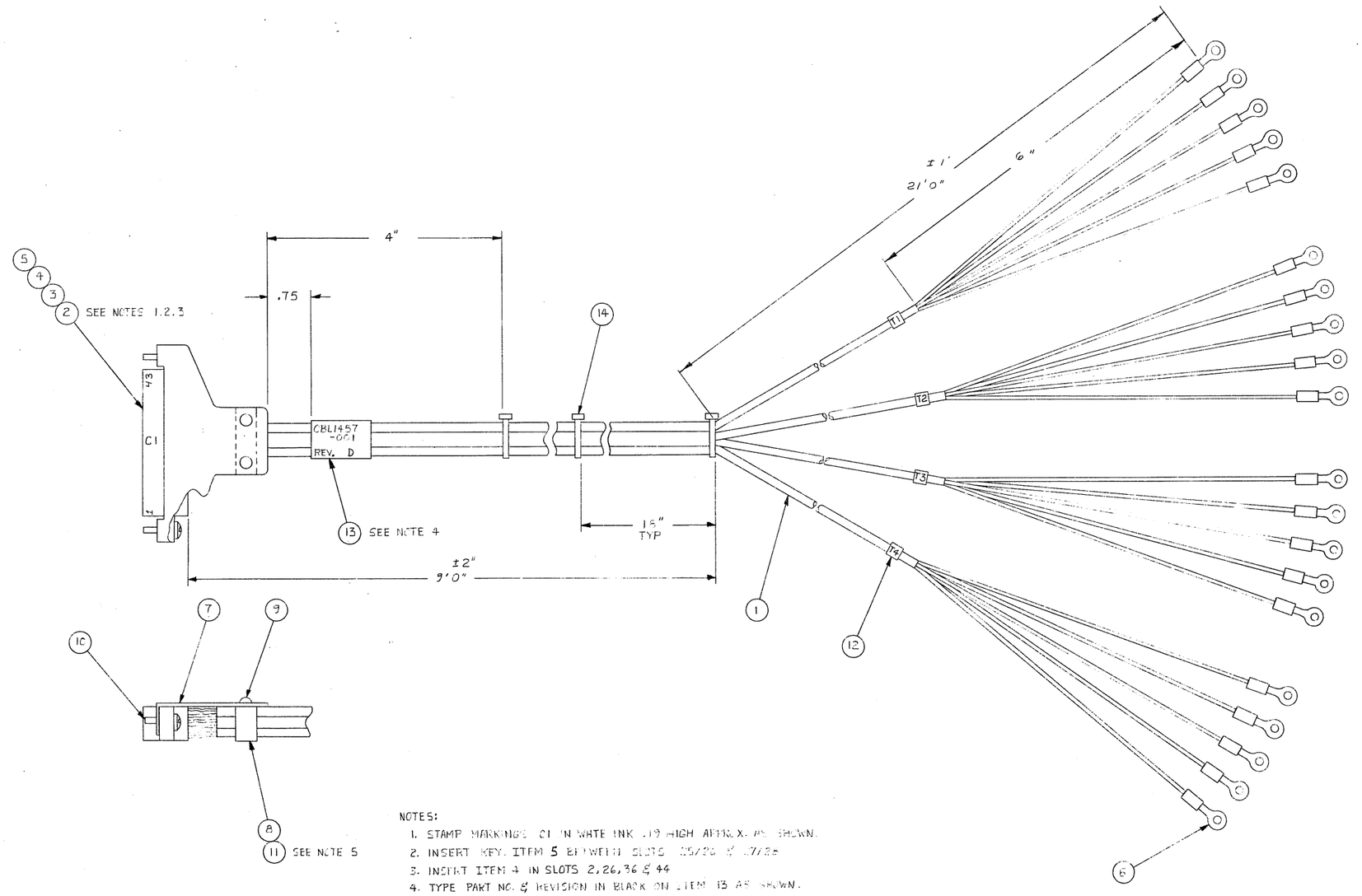
CABLE AMLC TO INFOTON CRT 4 EIA CONNECTORS

SCALE	SIZE	DWG. NO	REV.
SHEET OF	C	CBL1470-XXX	E

DWG. NO. CBL1470-XXX REV. E

WIRE LIST			
FROM	TO	COLOR	COMMENTS
C1-15	LUG	WHT	T1
C1-16	LUG	BROWN	
C1-33	LUG	RED	
C1-9	LUG	BLACK	
C1-29	LUG	GREEN	
C1-17	LUG	WHT	T2
C1-18	LUG	BROWN	
C1-35	LUG	RED	
C1-7	LUG	BLACK	
C1-27	LUG	GREEN	
C1-11	LUG	WHT	T3
C1-12	LUG	BROWN	
C1-39	LUG	RED	
C1-5	LUG	BLACK	
C1-25	LUG	GREEN	
C1-13	LUG	WHT	T4
C1-14	LUG	BROWN	
C1-41	LUG	RED	
C1-1	LUG	BLACK	
C1-23	LUG	GREEN	

LTR	DATE	REVISION	DR.	CK.
A	7-11-74	RELEASED	RK	JCL
B	12-16-74	REVISED PER ECN 1504	WB	JCL
C	4/29/75	PER ECN 1584	WB	JCL
D	7/15/75	PER ECN 1628	WB	JCL



NOTES:

1. STAMP MARKINGS (1) IN WHITE INK .10 HIGH APPROX. AS SHOWN.
2. INSERT KEY, ITEM 5 BETWEEN SLOTS 25/26 & 27/28
3. INSERT ITEM 4 IN SLOTS 2,26,36 & 44
4. TYPE PART NO. & REVISION IN BLACK ON ITEM 13 AS SHOWN.
5. INSTALL ITEM 11 IN CUTOUT OF ITEM 5 TO INSURE TIGHT FIT OF APPLE
6. FOR 20mA CURRENT LOOP - BROWN LEAD NOT USED
7. WHEN ALPHA WIRE IS USED THE BROWN WIRE IS ORANGE.

MATERIAL: SEE BOM	DWN: K.T. LENK	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK: [illegible]	CABLE ASSY, AMLC TO RING TONGUE TERMINATIONS
	ENG: [illegible]	
	APPRD: [illegible]	
	USED ON	SCALE NONE · SIZE D · DWG. NO. CBL1457-001 · REV. D
	NEXT ASSY 3161-003	SHEET 1 OF 1

DWG. NO. CBL1457-001 REV. D

PRIME COMPUTER INC.
NATICK MASS.

DWN. D.F. Gray
CHK. J.C. 4/1/74
ENG. [illegible] 4/1/74
APPRD. [illegible]
STANDARD COST _____ DATE _____

TITLE: AMLC FOR 103 / 102 DATA SETS 8 LINES

BOM 5002-XXX REV. H
NHA: — SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
B	REL	—	F	1597	[illegible]
C	1384	[illegible]	G	1617	[illegible]
D	1407	[illegible]	H	PNC 9/10	[illegible]
E	1411/1429	[illegible]			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1	D	2078-901	1								AMLC ASS'Y, 8L E.V.	A
2	D	2068-901	1								DATA SET CONTROL, W.W.	
												A
												A

PDF-004

PRIME COMPUTER INC.
NATICK MASS.

DWN. D.F. Gray
CHK. J.C. 4/1/74
ENG. [illegible]
APPRD. [illegible]
STANDARD COST _____ DATE _____

TITLE: AMLC FOR 103 / 102 DATA SETS 16 LINES

BOM 5004-XXX REV. H
NHA: — SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
B	REL	—	F	1597	[illegible]
C	1384	[illegible]	G	1617	[illegible]
D	1407	[illegible]	H	PNC 9/10	[illegible]
E	1411/1429	[illegible]			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1	D	2078-902	1								AMLC ASS'Y, 16 L E.V.	A
2	D	2068-902	1								DATA SET CONTROL W.W.	
												A
												A

PDF-004

PRIME COMPUTER INC.
NATICK MASS.

DWN. D.F. Gray
CHK. [illegible] 2/5/74
ENG. [illegible]
APPRD. [illegible]
STANDARD COST _____ DATE _____

TITLE: DATA SET CONTROL ASS'Y W.W. BOARD

BOM 2068-XXX REV. E
NHA: 5002 & 5004 SHT. 1 OF 2

REV.	ECN	CK	REV.	ECN	CK
B	REL	—	D1	1726	[illegible]
C	1333	[illegible]	E	PNC 9/10	[illegible]
D	1429	[illegible]			
D1	1451	[illegible]			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1	D	ESA2009-901	1	1							P.C. BD. SOCKET ASS'Y, D.S.C.	A
2	C	MEC0587	1	1							STIFFENER ASS'Y	
3	C	MEC0270	1	1							PINFIELD GUARD	
4	A	MEC0412	4	4							STAND-OFF, PINFIELD GUARD	
5		MEC0303-004	10	10							SCREW, RD.HD. NYLON, #4-40 X 1/4 LG	
6		MEC0303-005	5	5							SCREW, PAN HEAD, #4-40 X 5/16 LG	
7		MEC0356	5	5							WASHER, FLAT FIBER	A
8		MEC0388-002	5	5							NUT, SELF LOCKING #4-40	
9		ICD0135	2	4							7404	
10		ICD0191	2	4							7408	
11		ICD0049	4	8							74153	
12		ICD0050	2	4							74155	
13		ICD0054	8	16							74175	
14		ICD0112	2	4							8095	
15		ICD0067	8	16							1488	
16		ICD0068	8	16							1489	
17	A	MEC1248-022	4	8							CAPACITOR DIP ASS'Y C22	
18	A	MEC1264-016	2	4							JUMPER DIP ASS'Y W16	
19	A	MEC0292	1	1							LABEL, MODEL & SERIAL NO.	
20		ICD0034	2	2							74H21	A
21		RES0250-153	1	1							RESISTOR NET 15K Ω R1	A
22	B	MEC 2370-001	1	1							LABEL, ECN LOG	A

78 141

PDF-004

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. [illegible] 2/5/74
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: DATA SET CONTROL ASS'Y W.W. BOARD

BOM 2068 -XXX REV. E
NHA: SHT. 2 OF 2

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-03	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
23	B	MEC 1590-004	2	4							LABEL, I/O CONN. IDENTIFICATION	

PDF-004A

PRIME COMPUTER INC. NATICK MASS.

DWN. P.B. 10/6/74 | CHK. [illegible] | ENG. [illegible] 10-9-75 | APPRD.

STANDARD COST _____ DATE _____

TITLE: AMLC BOARD ASSY FOR DSC E.V.
901: 8 LINES
902: 16 LINES

BOM 2078 -XXX REV. E/F

NHA: 5004-002 SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
A	REL		D	1723-A	
A.	1604		D.	1726	
B	1609/1614		E	1871	
C	1654		E/F	1894/1898/1914	

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	PCB1734-001	1	1							PC BOARD, AMLC	
2	C	MEC0587	1	1							STIFFENER ASSY, PC BD.	
3		MEC0303-005	5	5							SCREW, PAN HEAD, 4-40 X 5/16 LG	2A
4		MEC0356	10	10							WASHER, FLAT FIBRE #4	
5		MEC0388-002	5	5							NUT, SELF LOCKING 4-40	
6	B	MEC1406-001	9	9							BUS BAR, INSULATED	
7		WIR1365-004	A/R	A/R							WIRE, 30 AWG YELLOW	
8		CAP0129	124	142							CAPACITOR, CER DISK .01MF, 25V	
9	B	MEC1590-006	1	1							I/O CONN IDENTIFICATION	2A
10		XTL0697	1	1							OSCILLATOR, 7.372800HZ	
11		ICD0025	6	6							74H00	
12		ICD0026	2	2							74H01	
13		ICD0028	12	12							74H04	
14		ICD0029	5	5							74H08	
15		ICD0030	4	4							74H10	
16		ICD0031	4	4							74H11	
17		ICD0033	2	2							74H20	
18		ICD0034	2	2							74H21	
19		ICD0035	2	2							74H30	
20		ICD0037	1	1							74H40	
21		ICD0038	2	2							74H50	
22		ICD0040	1	1							74H53	

PBF-004A REVISION

PRIME COMPUTER INC. NATICK MASS.

DWN. P.B. 10/4/74 | CHK. | ENG. | APPRD.

STANDARD COST _____ DATE _____

TITLE: AMLC BOARD ASSY. FOR DSC
-901: 8 LINES
-902: 16 LINES
E.V.

BOM 2078 -XXX REV. E/F

NHA: SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
23		ICD0043	2	2							74H74	
24		ICD0046	7	7							74H106	
25		ICD0048	10	18							74151	
26		ICD0049	24	29							74153	
27		ICD0050	2	2							74155	
28		ICD0051	5	5							74157	
29		ICD0052	15	15							74161	
30		ICD0053	17	24							74174	
31		ICD0054	7	8							74175	
32		ICD0055	1	1							74181	
33		ICD0058	4	4							7442	
34		ICD0059	1	1							8094	
35		ICD0060	4	4							8262	
36		ICD0067	2	4							1488	4A
37		ICD0068	2	4							1489A	4A
38		ICD0072	2	2							74S112	
39		ICD0083	1	1							74158	
40		ICD0112	8	9							8095	
41		ICD0148	13	16							7475	
42		ICD0183	1	1							82S41	
43		ICD0186	4	4							74154	
44		ICD0131	5	5							7408	

PBF-004A

PRIME COMPUTER INC. NATICK MASS.

DWN. P.B. 10/4/74 | CHK. | ENG. | APPRD.

STANDARD COST _____ DATE _____

TITLE: AMLC BOARD ASSY FOR DSC
-901: 8 LINES
-902: 16 LINES
E.V.

BOM 2078 -XXX REV. E/F

NHA: SHT. 3 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
45		ICD0194	3	4							7400	
46		ICD0195	12	15							7404	
47		ICD0136	1	1							7410	
48		ICD0582	7	6							8225	
49		ICD1256	8	16							1602	
50		RES0250-102	4	4							RESISTOR NETWORK 1KΩ	
51		RES0250-202	1	1							RESISTOR NETWORK 2KΩ	
52	A	MEC1901-020	1	1							PROM SET, AMLC GA	
53	A	MEC1901-021	1	1							PROM SET, AMLC GB	
54		CAP0552-315	4	4							CAPACITOR, TANT, 2.5 MF C1, C2, C35, C36	
55		CAP2290-031	8	16							CAP, MONO 330pf C3-C18	4A
56		RES0221-356	2	2							RESISTOR, M.F. 1/4W, 2%, 1K R4, R5	
57		RES0221-400	3	3							RESISTOR, M.F. 1/4W, 2%, 2K R2, R3, R99	
58		ICD0085	1	1							7485	
59		ICD0215	1	1							74H55	
60		RES0250-153	1	1							RESISTOR NETWORK 15K	4A
61	B	MEC1590-004	2	4							LABEL, I/O CONN. IDENTIFICATION	4A
62	A	JDA2769-916	1	1							JUMPER DIP ASSY W916	4A 4A
63	A	JDA2769-917	1	1							JUMPER DIP ASSY W917	4A 4A
	A	SPC1864	REF	REF							PRODUCT SPEC	
	C	LBD1735	REF	REF							LOGIC BLOCK DIAGRAM	

PBF-004A

C

PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B. 10-8-74 Electric
CHK. [illegible] 9/23/74
ENG. [illegible] 10-24-75
APPRD.
STANDARD COST_____ DATE_____

TITLE: AMLC ASSY 8 LINES E.V.

BOM 5052 **-XXX** REV. F
NHA: SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
A	REL		D	1654	MS
B	1513, 1713 1726	[illegible]	E	1723-A	[illegible]
C	1609	[illegible]	E1	1726	[illegible]
C1	1604	[illegible]	F	1803, 1816 2062	[illegible]

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1	D	PCB1734-001		1							PC BOARD, AMLC	
2	C	MEC0587		1							STIFFENER ASSY, PC BOARD	
3		MEC0303-005		5							SCREW, PAN HD, 4-40 X 5/16 LG	
4		MEC0356		10							WASHER, FLAT FIBRE #4	
5		MEC0388-002		5							NUT, SELF LOCKING 4-40	
6	B	MEC1406-001		9							BUS BAR, INSULATED	
7		WIR1365-000		A/R							WIRE, 30 AWG BLACK	
8		CAP0125		116							CAPACITOR, CER DISC .01μF, 25V	
9												
10		XTL0697		1							OSCILLATOR 7.372800 HZ	
11		ICD0025		6							74H00	
12		ICD0026		2							74H01	
13		ICD0028		12							74H04	
14		ICD0029		5							74H08	
15		ICD0030		4							74H10	
16		ICD0031		4							74H11	
17		ICD0033		2							74H20	
18		ICD0034		2							74H21	
19		ICD0035		2							74H30	
20		ICD0037		1							74H40	
21		ICD0038		2							74H50	
22		ICD0040		1							74H53	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B. 10/9/74
CHK.
ENG.
APPRD.
STANDARD COST_____ DATE_____

TITLE: AMLC ASSY 8 LINES E.V.

BOM 5052 **-XXX** REV. F
NHA: SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
23		ICD0043		2							74H74	
24		ICD0046		7							74H106	
25		ICD0048		10							7415I	
26		ICD0049		21							74153	
27		ICD0050		1							74155	
28		ICD0051		5							74157	
29		ICD0052		15							74161	
30		ICD0053		16							74174	
31		ICD0054		7							74175	
32		ICD0055		1							7481	
33		ICD0058		4							7442	
34		ICD0059		1							8094	
35		ICD0060		4							8262	
36		ICD0067		4							1488	
37		ICD0068		4							1489A	
38		ICD0072		2							745112	
39		ICD0083		1							7458	
40		ICD0112		7							8095	
41		ICD0148		8							7475	
42		ICD0183		1							82S41	
43		ICD0186		4							74154	
44		ICD0191		3							7408	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B. 9/9/74
CHK.
ENG.
APPRD.
STANDARD COST_____ DATE_____

TITLE: AMLC ASSY 8 LINES E.V.

BOM 5052 **-XXX** REV. F
NHA: SHT. 3 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
45		ICD0194		3							7400	
46		ICD0195		12							7404	
47		ICD0196		1							7410	
48		ICD0215		1							74H55	
49		ICD0582		6							8225	
50		ICD1256		A							1602	
51		RES0250-102		4							RESISTOR NETWORK 1KΩ	
52		RES0250-202		1							RESISTOR NETWORK 2KΩ	
53	A	MEC1301-060		1							PROM SET, AMLC GA	
54	A	MEC1301-021		1							PROM SET, AMLC GB	
55		CAP0552-315		4							CAP, TANT 3.3μF C1, C2, C35, C36	
56		CAP2290-031		16							CAP, MONO, 330 pF C3-C9, C18-C25, C34	Δ
57		RES0221-356		2							RESISTOR, M.F. 1/4W, 2%, 1K R4, R5	
58		RES0221-400		3							RESISTOR, M.F. 1/4W, 2%, 2K R2, R3, R39	
59		RES0250-153		1							RESISTOR NETWORK 15K	E
60	B	MEC1570-004		2							LABEL, I/O CONN IDENTIFICATION	E
61	A	JDA2769-916		1							JUMPER DIP ASSY W916	F
62	B	MEC1590-006		1							LABEL, MOD.NO/SER.NO./REV	F
	A	SPC 1864	REF								PRODUCT SPEC	
	C	LBD 1735	REF								LOGIC BLOCK DIAGRAM	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B. 10/2/74 | CHK. J.C. 1/31/75 | ENG. 1/31/75 | APPRD.
STANDARD COST ______ DATE ______

TITLE: AMLC CONTROLLER 16 LINES

E.V.

BOM 5054 -XXX | REV. G | NHA: | SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
A	REL		D	1620	
B	1572, 1573, 1575		E	1654	
C	1609		F	1723-A	
C	1604		F	1726	

ITEM	SIZE	PART NUMBER	QTY -001	QTY -902	QTY -003	QTY -004	QTY -005	QTY -006	QTY -007	QTY -008	DESCRIPTION	STANDARD COST
1	D	PCB1734-001		1							PC BOARD, AMLC	
2	C	MEC0587		1							STIFFENER ASSY, PC BD.	
3		MEC0303-005		5							SCREW, PAN HD, 4-40X5/16 LG	△
4		MEC0356		10							WASHER, FLAT FIBRE #4	
5		MEC0388-002		5							NUT, SELF LOCKING 4-40	
6	B	MEC1406-001		9							BUS BAR, INSULATED	
7		WIR1365-000		A/R							WIRE, 30 AWG BLACK	
8		CAP0129		136							CAPACITOR, CER DISK .01uf, 25V	
9												
10		XTL0697		1							OSCILLATOR, 7.372800HZ	
11		ICD0025		6							74H00	
12		ICD0026		2							74H01	
13		ICD0028		12							74H04	
14		ICD0029		5							74H08	
15		ICD0030		4							74H10	
16		ICD0031		4							74H11	
17		ICD0033		2							74H20	
18		ICD0034		2							74H21	
19		ICD0035		2							74H30	
20		ICD0037		1							74H40	
21		ICD0038		2							74H50	
22		ICD0040		1							74H53	

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IV-1

PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B. 10/2/74 | CHK. J.C. 1/31/75 | ENG. | APPRD.
STANDARD COST ______ DATE ______

TITLE: AMLC CONTROLLER 16 LINES

E.V.

BOM 5054 -XXX | REV. G | NHA: | SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK
G	1908/2133				

ITEM	SIZE	PART NUMBER	QTY -001	QTY -902	QTY -003	QTY -004	QTY -005	QTY -006	QTY -007	QTY -008	DESCRIPTION	STANDARD COST
23		ICD0043		2							74H74	
24		ICD0046		7							74H106	
25		ICD0048		18							74151	
26		ICD0049		29							74153	
27		ICD0050		1							74155	
28		ICD0051		5							74157	
29		ICD0052		15							74161	
30		ICD0053		24							74174	
31		ICD0054		7							74175	
32		ICD0055		1							74181	
33		ICD0058		4							7442	
34		ICD0059		1							8094	
35		ICD0060		4							8262	
36		ICD0067		8							1488	
37		ICD0068		8							1489A	
38		ICD0072		2							74S112	
39		ICD0083		1							74158	
40		ICD0112		8							8095	
41		ICD0148		16							7475	
42		ICD0183		1							82S41	
43		ICD0186		4							74154	
44		ICD0191		4							7408	△G

PDF-004A

PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B. 10/2/74 | CHK. J.C. 1/31/75 | ENG. | APPRD.
STANDARD COST ______ DATE ______

TITLE: AMLC CONTROLLER 16 LINES

E.V.

BOM 5054 -XXX | REV. G | NHA: | SHT. 3 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QTY -001	QTY -902	QTY -003	QTY -004	QTY -005	QTY -006	QTY -007	QTY -008	DESCRIPTION	STANDARD COST
45		ICD0194		4							7400	
46		ICD0195		15							7404	
47		ICD0196		1							7410	
48		ICD0582		6							8225	
49		ICD1256		16							1602	
50		RES0250-102		4							RESISTOR NETWORK 1KΩ	
51		RES0250-202		1							RESISTOR NETWORK 2KΩ	
52	A	MEC1901-020		1							PROM SET, AMLC GA	
53	A	MEC1901-021		1							PROM SET, AMLC GB	
54		CAP0552-315		4							CAPACITOR, TANT, 3.3uf C1, C2, C35, C36	
55		CAP2290-031		32							CAP, MONO 330pf C3-C34	△
56		RES0221-356		2							RESISTOR, M.F. 1/4W, 2%, 1K R4, R5	△G
57		RES0221-400		3							RESISTOR, M.F. 1/4W, 2%, 2K R2, R3, R99	
58		RES0250-153		1							RESISTOR NETWORK 15K	△F
59		ICD0215		1							74H55	△F
60	B	MEC1590-004		4							LABEL, I/O CONN. IDENTIFICATION	△F
61	A	JDA2769-916		1							JUMPER DIP ASSY W916	△G
	A	SPC1864		REF							PRODUCT SPEC	
	C	LBD1735		REF							LOGIC BLOCK DIAGRAM	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B. 12/30/75
CHK. [illegible] 12/31/75
ENG. [illegible]
APPRD.
STANDARD COST _____ DATE _____

TITLE: AMLC ASSY
8 LINES @ 20MA
(CURRENT LOOP)
E.V.

BOM 5072 -XXX REV. B
NHA: SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
A	REL	[illegible]			
A1	1723-A	[illegible]			
A2	1726	[illegible]			
B	1768/1760	[illegible]			

ITEM	SIZE	PART NUMBER	QUANTITY -901	DESCRIPTION	STANDARD COST
1	D	PCB1734-001	1	PC BOARD, AMLC	
2	C	MEC0587	1	STIFFENER ASSY PC BOARD	
3		MEC0303-005	5	SCREW, PAN HD, 4-40X5/16LG	B
4		MEC0256	10	WASHER, FLAT FIBRE #4	
5		MEC0388-002	5	NUT, SELF LOCKING 4-40	
6	B	MEC1406-001	9	BUS BAR, INSULATED	
7		WIR1365-001	A/R	WIRE, 30 AWG BROWN	
8		CAP0129	140	CAPACITOR, CER DISC .01MF, 25V	
9	B	MEC1590-006	1	LABEL I/O CONN IDENTIFICATION	A
10		XTL0687	1	OSCILLATOR, 7.372800 HZ	
11		ICD0025	6	74H00	
12		ICD0026	2	74H01	
13		ICD0028	12	74H04	
14		ICD0029	5	74H08	
15		ICD0030	4	74H10	
16		ICD0031	4	74H11	
17		ICD0033	2	74H20	
18		ICD0034	2	74H21	
19		ICD0035	2	74H30	
20		ICD0037	1	74H40	
21		ICD0038	2	74H50	
22		ICD0039	1	74H53	

PBF-004A

PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B.
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: AMLC ASSY
8 LINES @ 20MA
(CURRENT LOOP)
E.V.

BOM 5072 -XXX REV. B
NHA: SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	DESCRIPTION	STANDARD COST
23		ICD0043	2	74H74	
24		ICD0046	7	74H106	
25		ICD0048	10	74151	
26		ICD0049	21	74153	
27		ICD0050	1	74155	
28		ICD0051	5	74157	
29		ICD0052	15	74161	
30		ICD0053	16	74174	
31		ICD0054	7	74175	
32		ICD0055	1	74181	
33		ICD0058	4	7442	
34		ICD0059	1	8094	
35		ICD0060	4	8262	
36					
37		ICD0068	2	1489A	
38		ICD0072	2	75112	
39		ICD0083	1	74158	
40		ICD0112	7	8095	
41		ICD0113	2	7438	
42		ICD0148	8	7475	
43		ICD0183	1	82S41	
44		ICD0186	4	74154	

PBF-004A

PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B.
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: AMLC ASSY
8 LINES @ 20MA
(CURRENT LOOP)
E.V.

BOM 5072 -XXX REV. B
NHA: SHT. 3 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	DESCRIPTION	STANDARD COST
45		ICD0191	5	7408	
46		ICD0194	3	7400	
47		ICD0195	12	7404	
48		ICD0196	1	7410	
49		ICD0215	1	74H55	
50		ICD0582	6	9235	
51		ICD1256	8	1602	
52		RES0250-102	5	RESISTOR NETWORK 1K Ω	
53		RES0250-202	1	RESISTOR NETWORK 2K Ω	
54	A	MEC1301-020	1	PROM SET AMLC GA	
55	A	MEC1301-021	1	PROM SET AMLC GB	
56	A	MEC1288-015	2	RESISTOR DIP ASSY R15	
57	A	MEC1288-016	2	RESISTOR DIP ASSY R16	
58	B	MEC1590-004	2	LABEL, I/O CONN. IDENTIFICATION	A
59		CAP0552-315	4	CAP, TANT. 3.3MF C1, C2, C35 C36	
60		RES0221-356	2	RESISTOR, M.F. 1/4W 2%, 1K R4, R5	
61		RES0221-900	3	RESISTOR, M.F. 1/4W 2%, 2K R2, R3, R99	
62		RES0250-153	1	RESISTOR NETWORK 15K	A
63	A	JDA2769-916	1	JUMPER DIP ASSY W916	B
	A	SPC1864	REF	PRODUCT SPEC	
	C	LBD1735	REF	LOGIC BLOCK DIAGRAM	

PBF-004A

PRIME COMPUTER INC.
NATICK MASS.

DWN. R.B. 10-6-74 Bianchi
CHK. [illegible] 11/24/75
ENG. [illegible]
APPRD.
STANDARD COST _____ DATE _____

TITLE: AMLC ASSY
16 LINES @ 20MA
E.V.

BOM 5074 **-XXX** REV. F

NHA: SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
A	REL		D	1726	
B	1609		E	1928, 2116, 2154	
C	1725-4		F	2213	
D	1750, 1722-A				

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1	D	PCB1734-001		1							PC BOARD, AMLC	
2	C	MEC0587		1							STIFFENER ASSY, PC BOARD	
3		MEC0303-005		5							SCREW PAN HD, 4-40 X 5/16 LG	(E)
4		MEC0356		10							WASHER, FLAT FIBRE #4	
5		MEC0388-002		5							NUT, SELF LOCKING 4-40	
6	B	MEC1406-001		2							BUS BAR, INSULATED	
7		WIR1365-001		A/R							WIRE, 30 AWG BROWN	
8		CAP0129		140							CAPACITOR, CER DISC .01uF, 25V	
9	B	MEC1590-006		1							LABEL, MODEL NO./SER. NO./REV	(E)
10		XTL0697		1							OSCILLATOR 7.372800 MZ	
11		ICD0025		6							74H00	
12		ICD0026		2							74H01	
13		ICD0028		12							74H04	
14		ICD0029		5							74H08	
15		ICD0030		4							74H10	
16		ICD0031		4							74H11	
17		ICD0033		2							74H20	
18		ICD0034		2							74H21	
19		ICD0035		5							74H30	
20		ICD0037		1							74H40	
21		ICD0038		2							74H50	
22		ICD0040		1							74H53	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. R.B. 10/4/74
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: AMLC ASSY
16 LINES @ 20MA
E.V.

BOM 5074 **-XXX** REV. F

NHA: SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
23		ICD0043		2							74H74	
24		ICD0046		7							74H106	
25		ICD0048		18							74151	
26		ICD0049		29							74153	
27		ICD0050		1							74155	
28		ICD0051		5							74157	
29		ICD0052		15							74161	
30		ICD0053		24							74174	
31		ICD0054		7							74175	
32		ICD0055		1							74181	
33		ICD0058		4							7442	
34		ICD0059		1							8094	
35		ICD0060		4							8262	
36												
37		ICD0068		4							1489A	
38		ICD0072		2							74S112	
39		ICL0083		1							74158	
40		ICD0112		8							8095	
41		ICD0113		4							7438	
42		ICD0148		16							7475	
43		ICD0183		1							82S41	
44		ICL0186		4							74154	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. R.B. 10/4/74
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: AMLC ASSY
16 LINES @ 20MA
E.V.

BOM 5074 **-XXX** REV. F

NHA: SHT. 3 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
45		ICD0191		5							7408	
46		ICD0194		4							7400	
47		ICD0195		15							7404	
48		ICD0196		1							7410	
49		ICD0215		1							74H55	
50		ICD0582		6							8235	
51		ICD1256		16							8602	
52		RES0250-102		6							RESISTOR NETWORK 1K Ω	
53		RES0250-202		1							RESISTOR NETWORK 2K Ω	
54	A	MEC1301-020		1							PROM SET GA	
55	A	MEC1301-021		1							PROM SET GB	
56	A	MEC1288-015		4							RESISTOR DIP ASSY R15	
57	A	MEC1288-016		4							RESISTOR DIP ASSY R16	
58	B	MEC1590-004		4							LABEL, I/O CONN. IDENTIFICATION	(D)
59		CAP0552-3.3		4							CAP, TANT. 3.3uF C1, C2, C35, C36	
60		RES0221-856		2							RESISTOR, M.F. 1/4W 2%, 1K R4, R5	
61		RES0221-900		3							RESISTOR, M.F. 1/4W 2%, 2K R2, R3, R99	
62		RES0250-163		1							RESISTOR NETWORK 15K	(D)
63		JDA2769-916		1							JUMPER DIP ASSY W916	(E)
	A	SPC 1964		REF							PRODUCT SPEC	
	C	LBD1735		REF							LOGIC BLOCK DIAGRAM	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B. 10-4-74
CHK. # 12-23-74
ENG. 12.6.75
APPRD.
STANDARD COST _____ DATE _____

TITLE: AMLC ASSY
8 LINES @ 20 MA
8 LINES @ RS232
E.V.

BOM 5075 **-XXX** REV. 6
NHA: SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
A	REL		D	1654	
B	1594		E	1723-A	
C	1609		E1	1726	
C1	1604		F	1808 12/23/2116	

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1	D	PCB1734-001		1							PC BOARD, AMLC	
2	C	MEC0587		1							STIFFENER ASSY, PC BOARD	
3		MEC0303-005		5							SCREW, PAN HEAD, 4-40X5/16LG	A
4		MEC0356		10							WASHER, FLAT FIBRE #4	
5		MEC0388-002		5							NUT, SELF LOCKING 4-40	
6	B	MEC1406-001		9							BUS BAR, INSULATED	
7		WIR1365-001		A/R							WIRE, 30 AWG BROWN	
8		CAP0129		140							CAPACITOR, CER DISC .01μf, 25V	
9	B	MEC1590-006		1							LABEL, MOD. NO./SER. NO./REV	A
10		XTL0687		1							OSCILLATOR, 7.372800 HZ	
11		ICD0025		6							74H00	
12		ICD0026		2							74H01	
13		ICD0028		12							74H04	
14		ICD0029		5							74H08	
15		ICD0030		4							74H10	
16		ICD0031		4							74H11	
17		ICD0033		2							74H20	
18		ICD0034		2							74H21	
19		ICD0035		2							74H30	
20		ICD0037		1							74H40	
21		ICD0038		2							74H50	
22		ICD0040		1							74H53	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B. 10/4/74
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: AMLC ASSY
8 LINES @ 20MA
8 LINES @ RS232
E.V.

BOM 5075 **-XXX** REV. 6
NHA: SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK
G	2214				

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
23		ICD0043		2							74H74	
24		ICD0046		7							74H106	
25		ICD0048		18							74151	
26		ICD0049		29							74153	
27		ICD0050		1							74155	
28		ICD0051		5							74157	
29		ICD0052		15							74161	
30		ICD0053		24							74174	
31		ICD0054		7							74175	
32		ICD0055		1							74181	
33		ICD0058		4							7442	
34		ICD0059		1							8094	
35		ICD0060		4							8262	
36		ICD0067		4							1488	
37		ICD0068		6							1489A	
38		ICD0072		2							74S112	
39		ICD0083		1							74158	
40		ICD0112		8							8095	
41		ICD0113		2							7438	
42		ICD0148		16							7475	
43		ICD0183		1							82S41	
44		ICD0186		4							74154	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. P.B. 10/4/74
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: AMLC ASSY
8 LINES @ 20 MA
8 LINES @ RS232
E.V.

BOM 5075 **-XXX** REV. G
NHA: SHT. 3 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
45		ICD0191		5							7408	
46		ICD0194		4							7400	
47		ICD0195		15							7404	
48		ICD0196		1							7410	
49		ICD0215		1							74H55	
50		ICD0582		6							8225	
51		ICD1256		16							1602	
52		RES0250-102		5							RESISTOR NETWORK 1KΩ	
53		RES0250-202		1							RESISTOR NETWORK 2KΩ	
54	A	MEC1901-020		1							PROM SET AMLC	
55	A	MEC1901-021		1							PROM SET AMLC	
56	A	MEC1288-015		2							RESISTOR DIP ASSY R15	
57	A	MEC1288-016		2							RESISTOR DIP ASSY R16	
58		CAP2290-031		16							CAP, MONO, 330pf C10-C17, C26-C33	A
59		CAP0552-315		4							CAP, TANT. 3.3μf C1, C2, C35, C36	
60		RES0221-356		2							RESISTOR, M.F. 1/4W 2% 1K R4, R5	
61		RES0221-400		3							RESISTOR, M.F 1/4W 2% 2K R2, R3, R99	
62		RES0250-153		1							RESISTOR NETWORK 15K	A
63	B	MEC1390-004		4							LABEL, I/O CONN. IDENTIFICATION	A
64	A	VCA2769-3/6		1							JUMPER DIP ASSY W9/6	A
	A	SPC 1864		REF							PRODUCT SPEC	
	C	LED1735		REF							LOGIC BLOCK DIAGRAM	

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